

Compal Confidential

Model Name :Q5WV1/Q5WS1

Compal Project Name :

File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document

Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH

Nvidia N13P GS/GL

2012-02-03b

REV : 0 . 3

MB PCB

Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B

ZZZ2 1G@



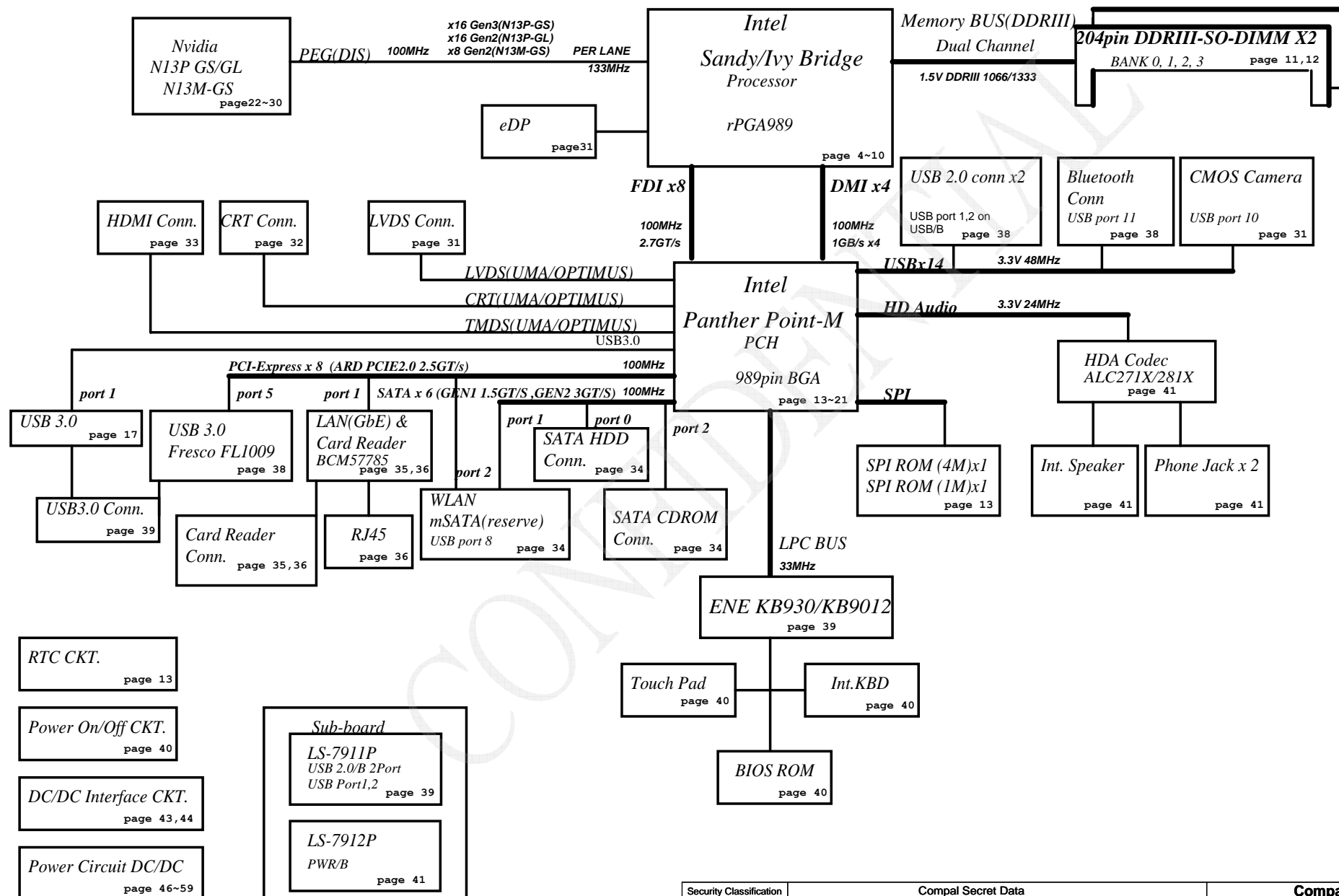
X76344BOL01

ZZZ3 2G@



X76344BOL02

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power rail for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b		

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

4319IDBOL01SMT MB A7912 Q5WV1 HM77 QC UMA 3
4319IDBOL02SMT MB A7912 Q5WV1 HM77 QC 13PGL1G 3
4319IDBOL03SMT MB A7912 Q5WV1 HM77 QC 13PGL2G 3
4319IDBOL04SMT MB A7912 Q5WV1 HM77 QC 13PGS1G 3
4319IDBOL05SMT MB A7912 Q5WV1 HM77 QC 13PGS2G 3
4319IDBOL06SMT MB A7912 Q5WV1 HM77 DC UMA 2
4319IDBOL07SMT MB A7912 Q5WV1 HM77 DC UMA 3
4319IDBOL08SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 2
4319IDBOL09SMT MB A7912 Q5WV1 HM77 DC 13PGL1G 3
4319IDBOL10SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 2
4319IDBOL11SMT MB A7912 Q5WV1 HM77 DC 13PGL2G 3
4319IDBOL12SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 2
4319IDBOL13SMT MB A7912 Q5WV1 HM77 DC 13MGS1G 3
4319IDBOL14SMT MB A7912 Q5WV1 HM77 DC 13PGS2G 3

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB3@
Internal USB 2.0	PUSB@
USB 2.0 flag	PUSB2@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@
N13P-GS & GL	GSGL@
N13M-GS	GM@
support AC function	AC@
no AC function	NOAC@

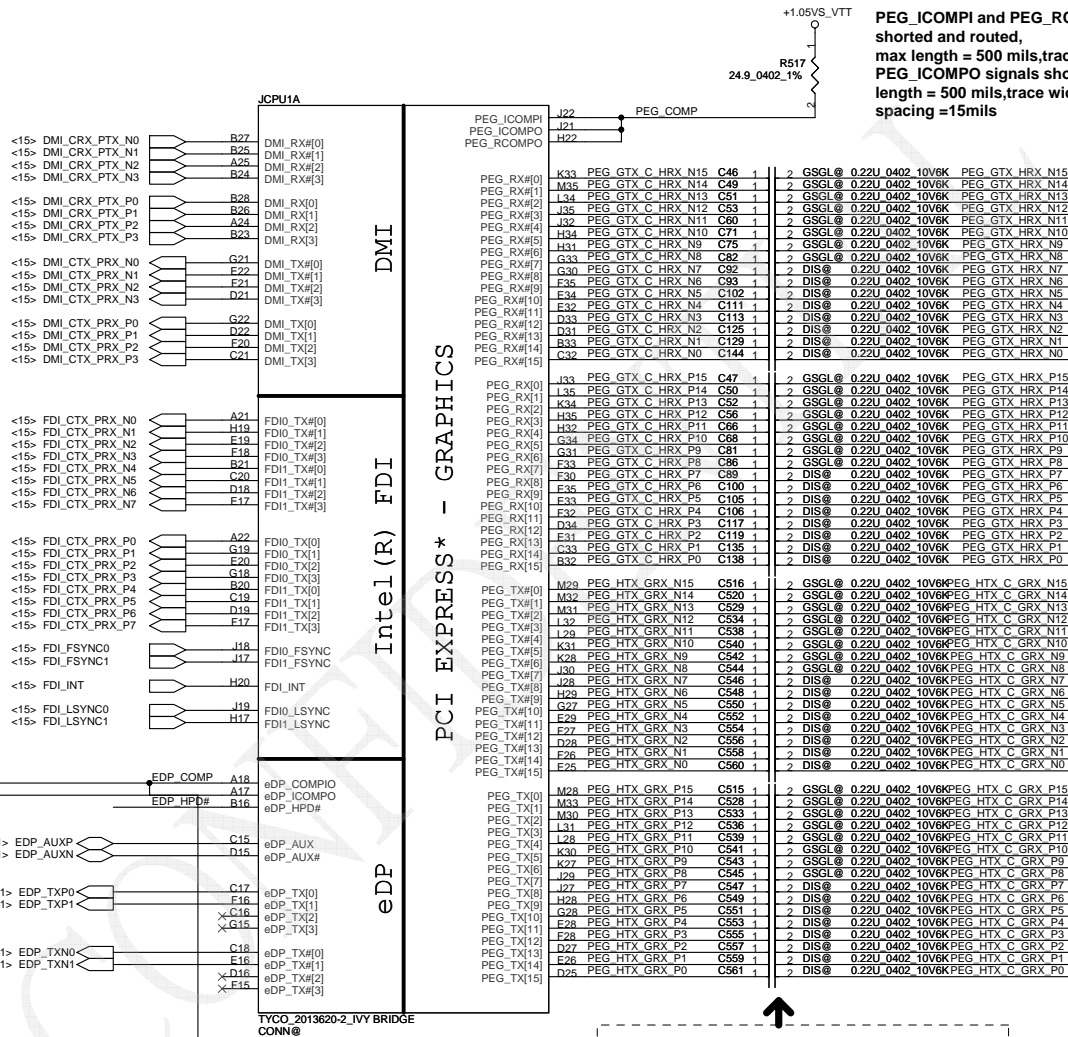
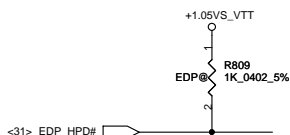
USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
		2	USB/B (Right Side)
	UHCI1	3	
		4	
	UHCI2	5	
EHCI2	UHCI3	6	
		7	
	UHCI4	8	Mini Card 1(WLAN)
		9	
	UHCI5	10	Camera
		11	BlueTooth
	UHCI6	12	
		13	

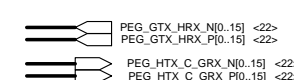
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eDP_COMPIO and ICOMPO signals should be shorted near balls, Trace Width for EDP_COMPIO=4mils, EDP_ICOMPO=12mils, and both length less than 500 mils... should not be left floating ,even if disable eDP function...

Add eDP circuit

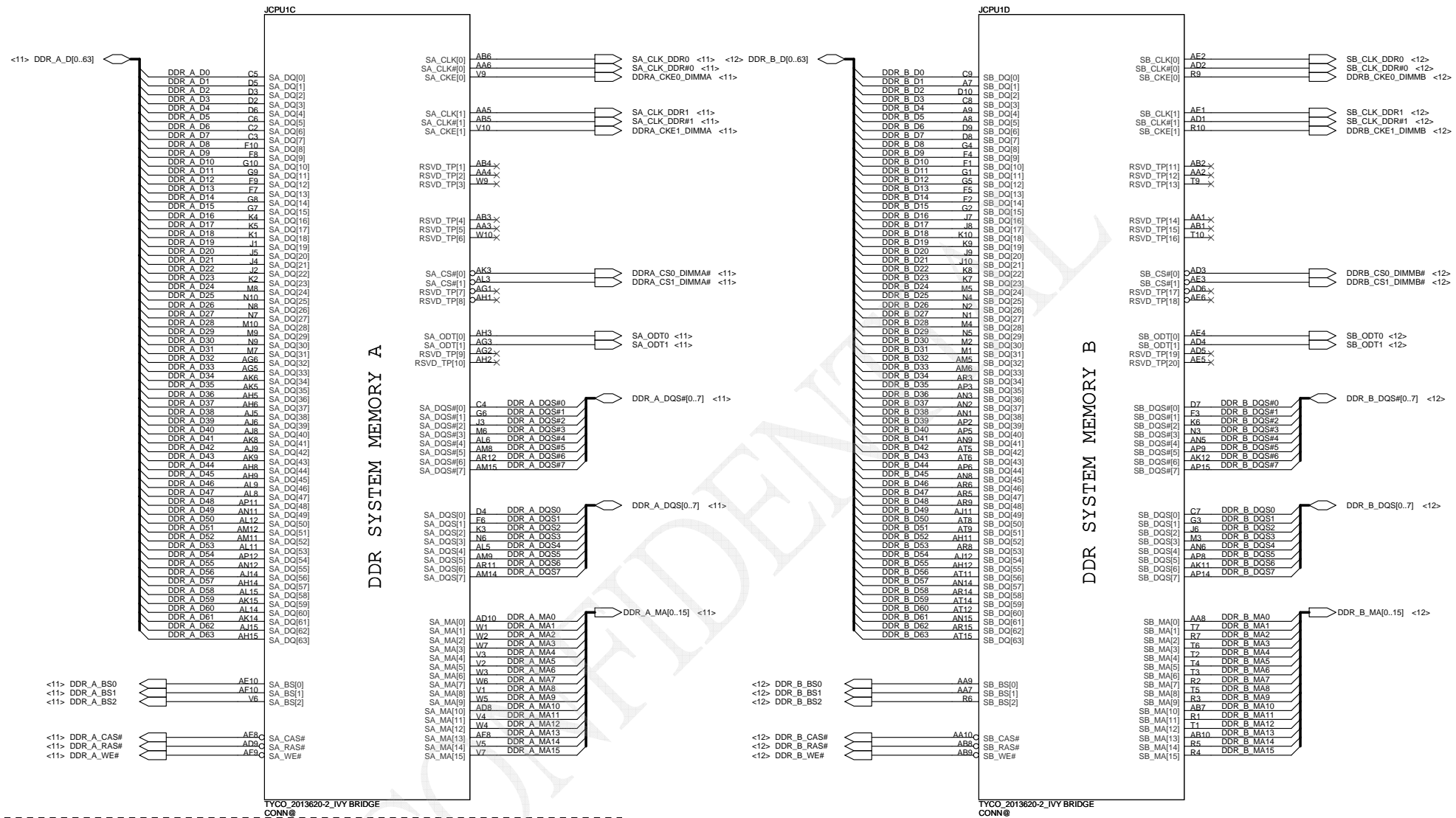


PEG_ICOMPI and PEG_RCOMPO signals should be shorted and routed, max length = 500 mils, trace width=4mils PEG_ICOMPO signals should be routed with - max length = 500 mils, trace width=12mils spacing =15mils



Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

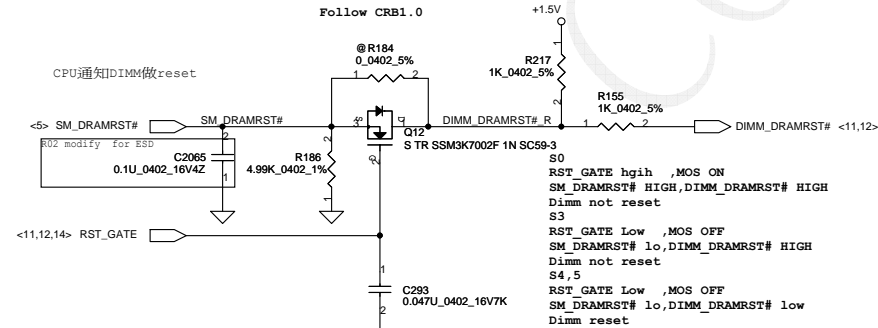
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TYCO_2013620-2_IVY BRIDGE
CONN@

TYCO_2013620-2_IVY BRIDGE
CONN@

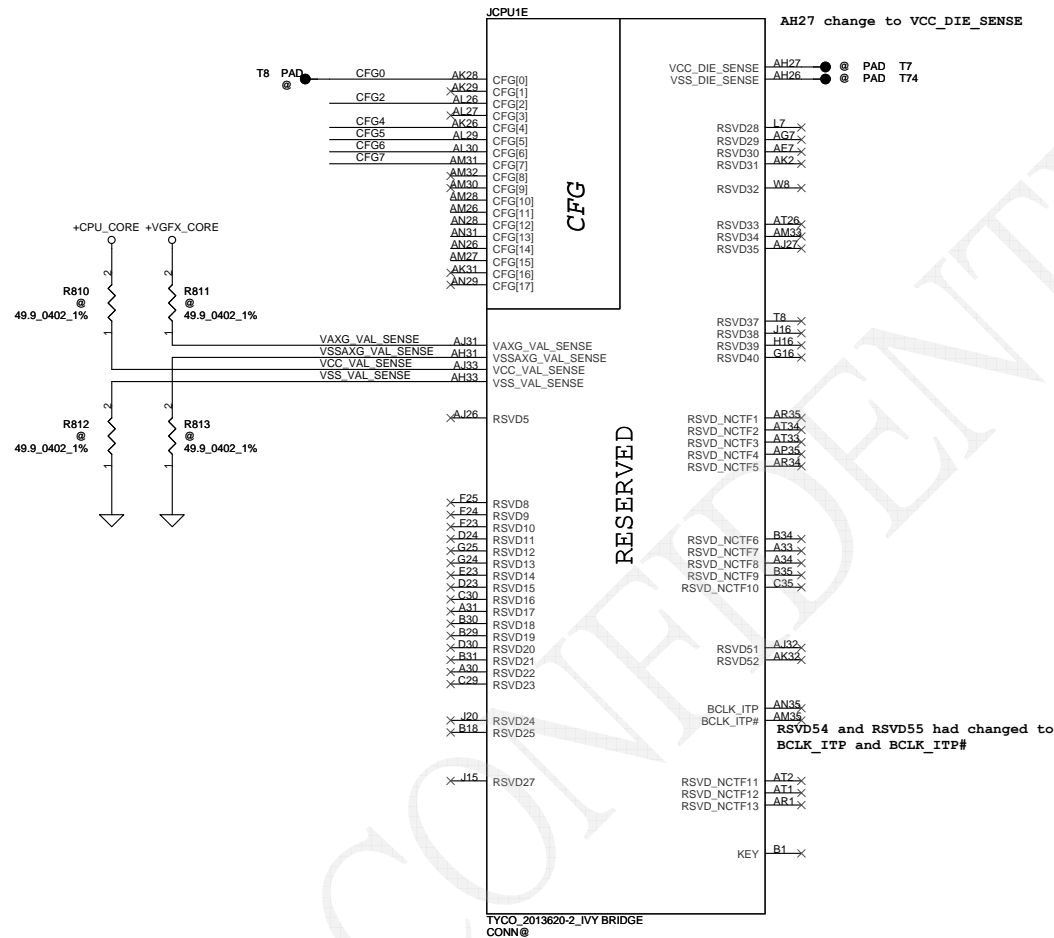
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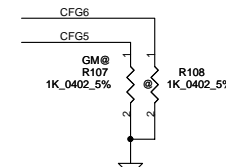
CFG Straps for Processor

AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE

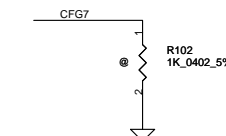


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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SV type CPU

JCPU1F

POWER

+CPU_CORE

QC 53A
DC 53A

8.5A

+1.05VS_VTT

PEG AND DDR

CORE SUPPLY

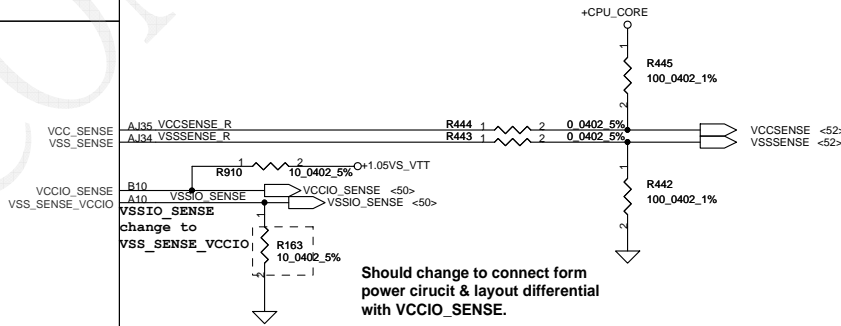
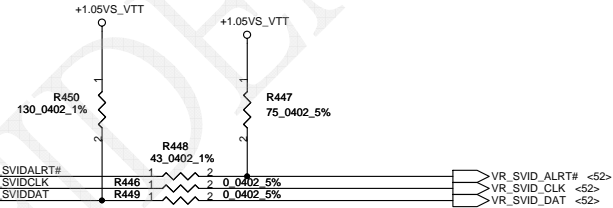
SVID

SENSE LINES

TYCO_2013620-2_IVY BRIDGE CONN@

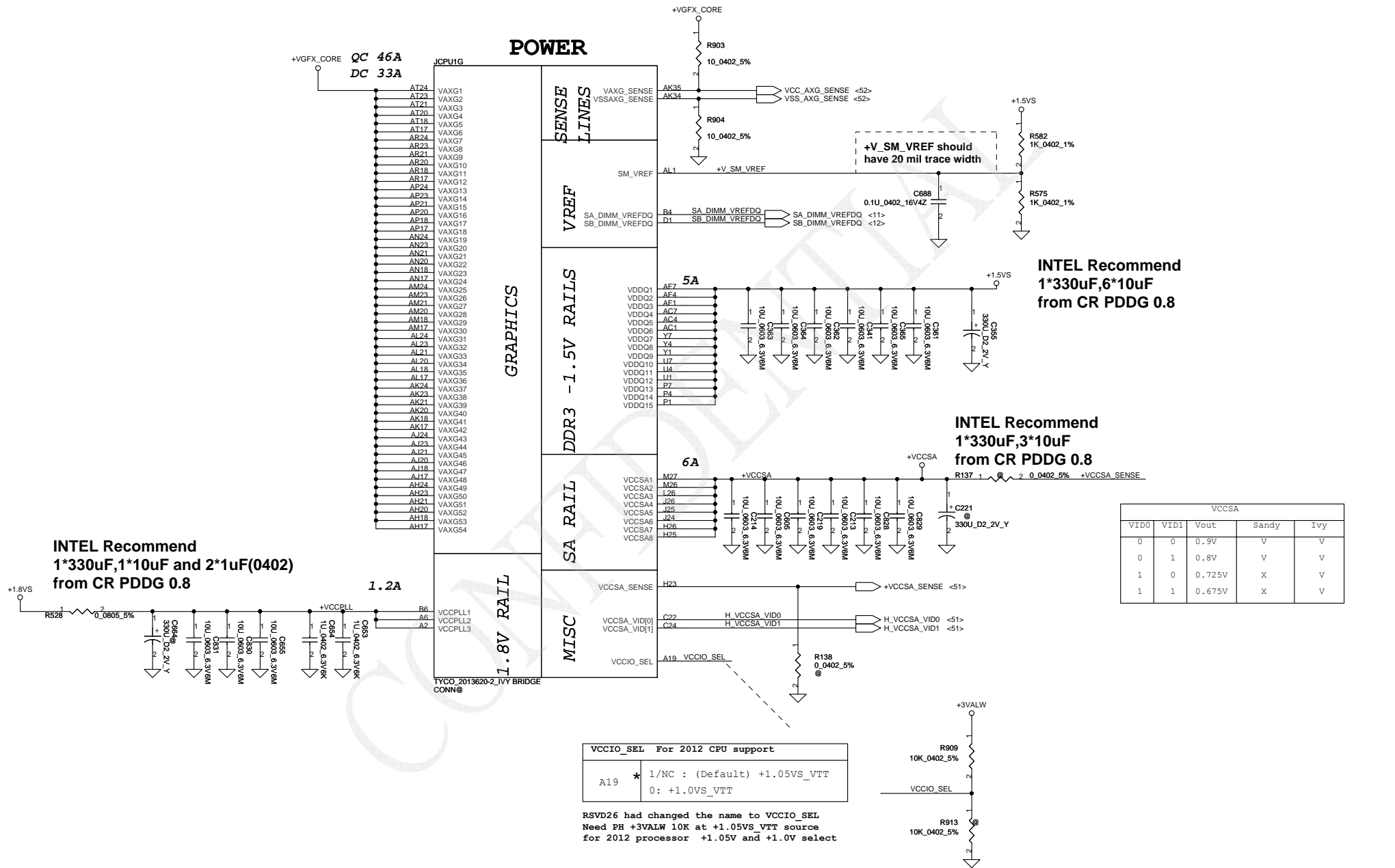
VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AC10
VCCIO4 Y10
VCCIO5 U10
VCCIO6 P10
VCCIO7 L10
VCCIO8 J14
VCCIO9 J13
VCCIO10 J12
VCCIO11 H14
VCCIO12 H14
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
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VCCIO37 A14
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VCCIO40 A11
J23

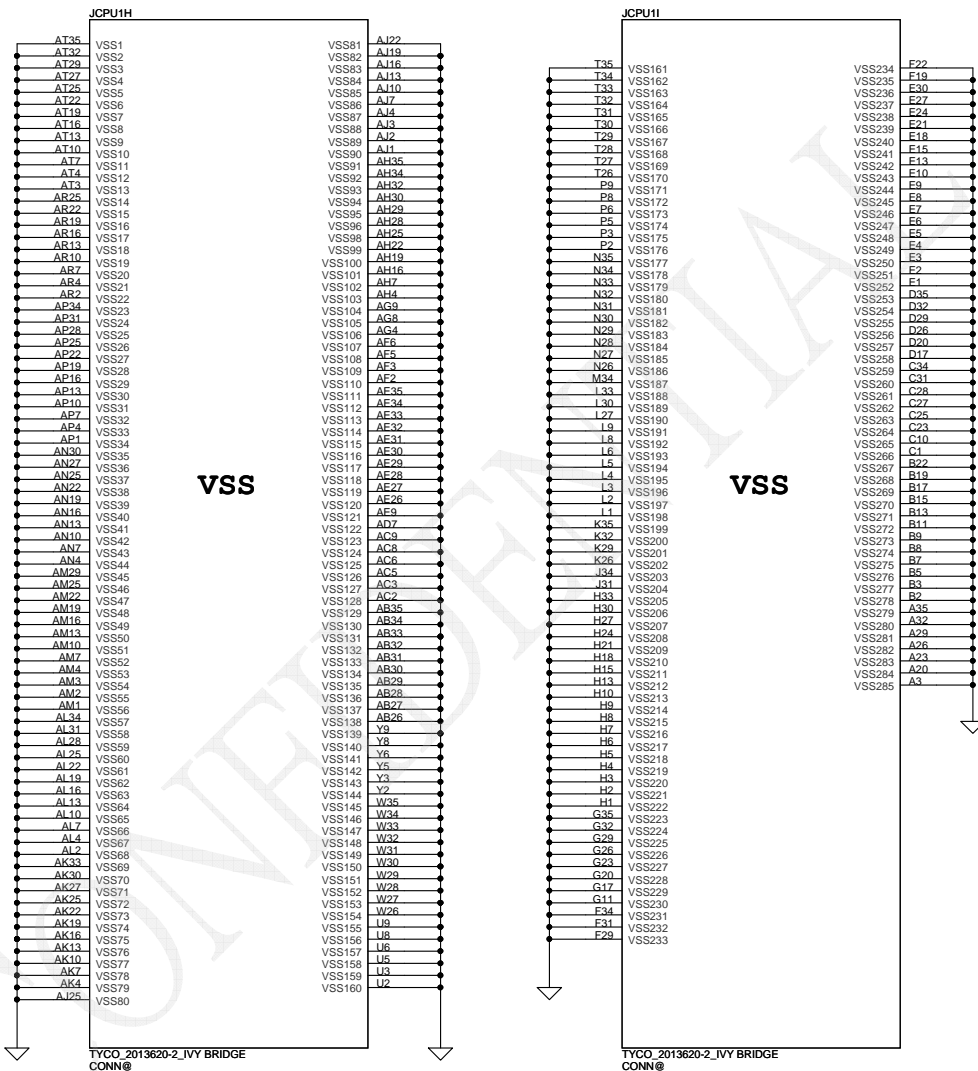
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VCC4 AG32
VCC5 AG31
VCC6 AG30
VCC7 AG29
VCC8 AG28
VCC9 AG27
VCC10 AG26
VCC11 AF35
VCC12 AF34
VCC13 AF33
VCC14 AF32
VCC15 AF31
VCC16 AF30
VCC17 AF29
VCC18 AF28
VCC19 AF27
VCC20 AF26
VCC21 AD35
VCC22 AD34
VCC23 AD33
VCC24 AD32
VCC25 AD31
VCC26 AD29
VCC27 AD28
VCC28 AD27
VCC29 AD26
VCC30 AC35
VCC31 AC34
VCC32 AC33
VCC33 AC32
VCC34 AC31
VCC35 AC30
VCC36 AC29
VCC37 AC28
VCC38 AC27
VCC39 AC26
VCC40 AA35
VCC41 AA34
VCC42 AA33
VCC43 AA32
VCC44 AA31
VCC45 AA30
VCC46 AA29
VCC47 AA28
VCC48 AA27
VCC49 AA26
VCC50 Y35
VCC51 Y34
VCC52 Y33
VCC53 Y32
VCC54 Y31
VCC55 Y30
VCC56 Y29
VCC57 Y28
VCC58 Y27
VCC59 Y26
VCC60 V35
VCC61 V34
VCC62 V33
VCC63 V32
VCC64 V31
VCC65 V29
VCC66 V28
VCC67 V27
VCC68 V26
VCC69 U35
VCC70 U34
VCC71 U33
VCC72 U32
VCC73 U31
VCC74 U30
VCC75 U29
VCC76 U28
VCC77 U27
VCC78 U26
VCC79 R35
VCC80 R34
VCC81 R33
VCC82 R32
VCC83 R31
VCC84 R30
VCC85 R29
VCC86 R28
VCC87 R27
VCC88 R26
VCC89 P35
VCC90 P34
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VCC100

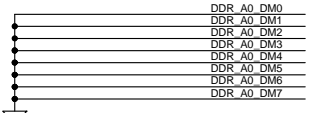
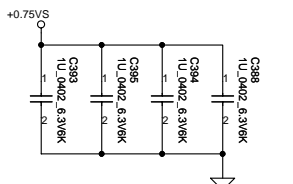
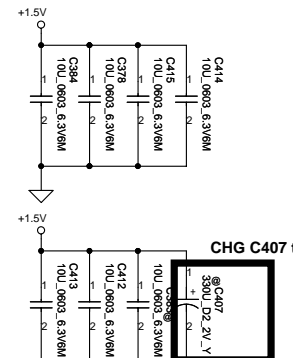
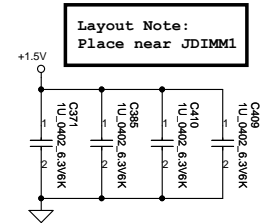
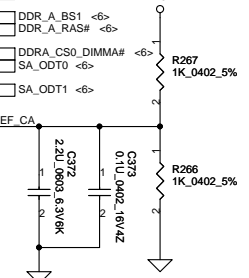
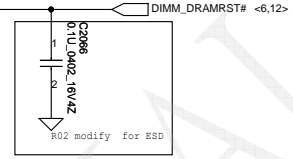
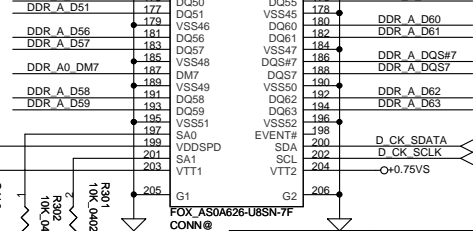
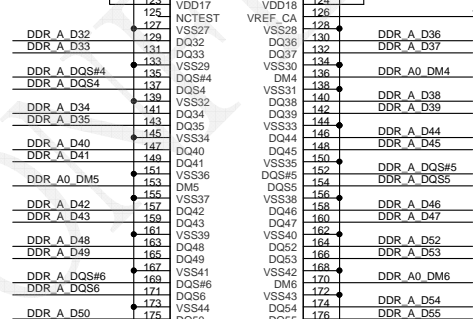
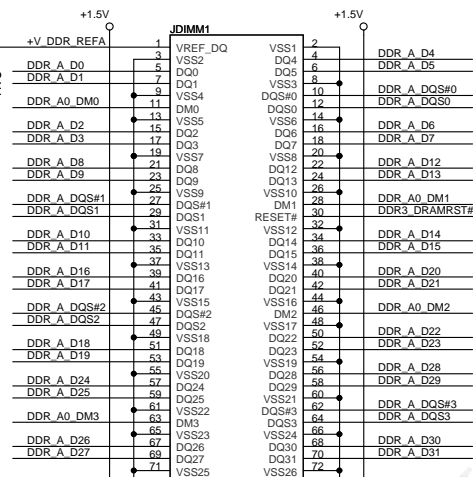
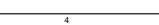
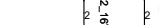
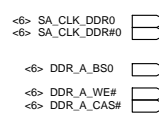
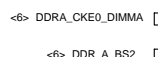
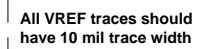
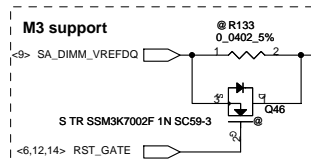


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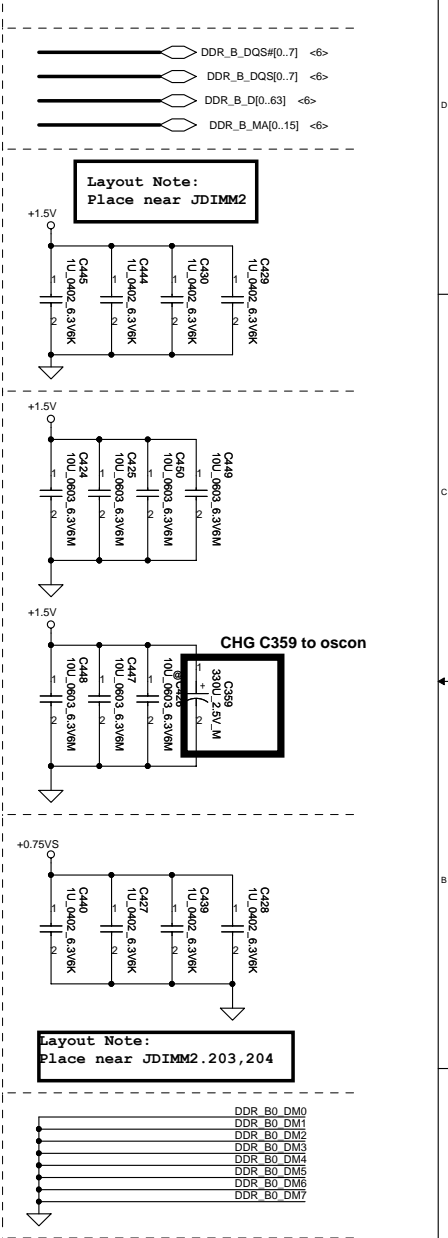
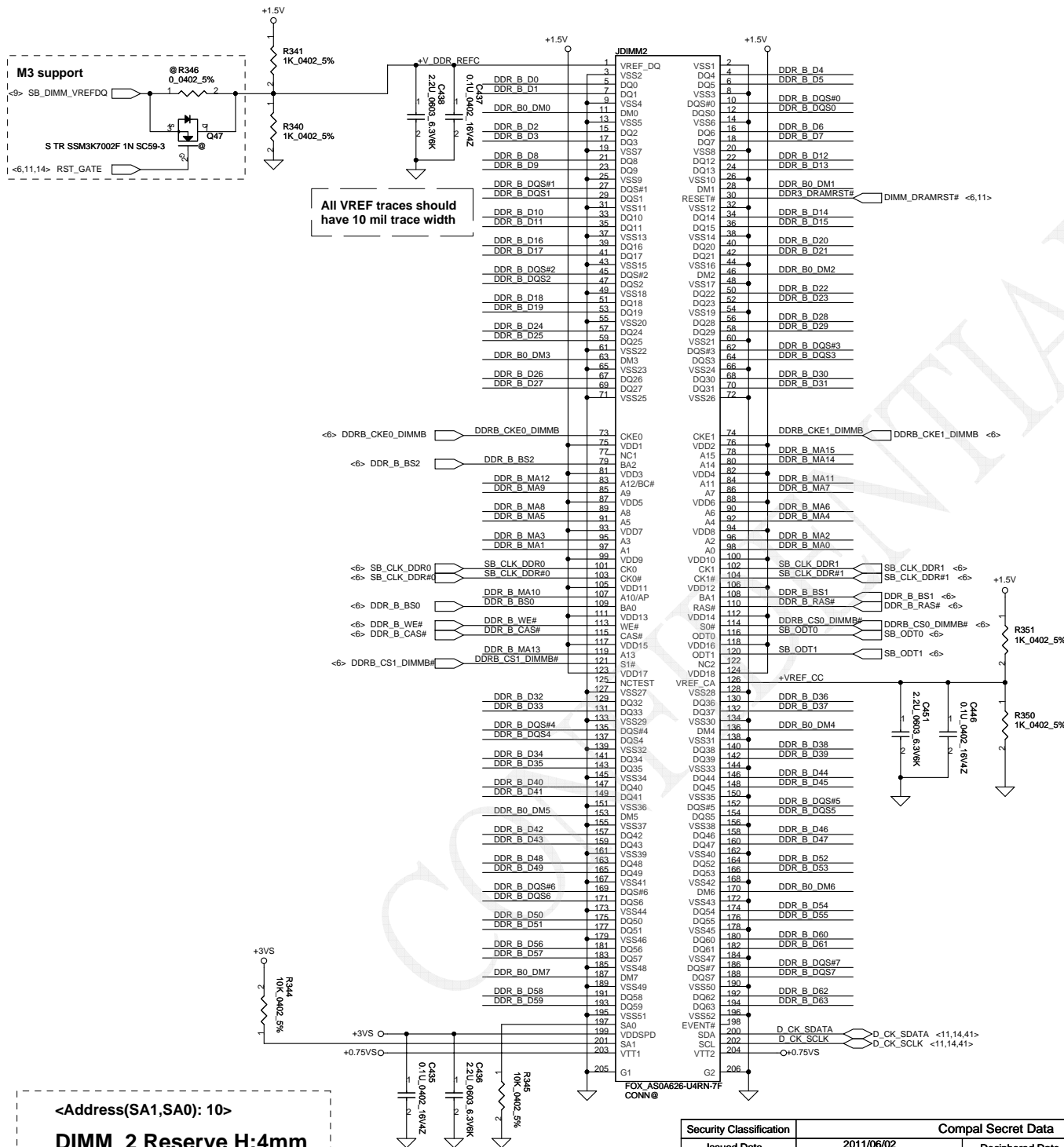




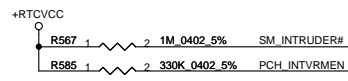


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DIMM_1 Reserve H:8mm

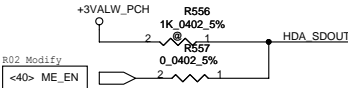
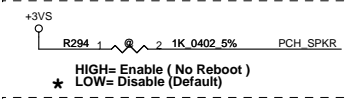
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				4019ID	
Date:	Friday, February 10, 2012	Sheet	11	of	83



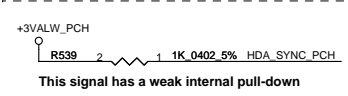
Security Classification		Compal Secret Data				
Issued Date	2011/06/02	Deciphered Date	2012/06/02	Title		
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				Document Number		Rev C
				40191D		
Date:				Friday, February 10, 2012	Sheet 12 of 63	



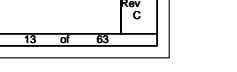
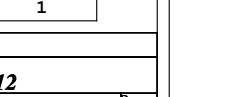
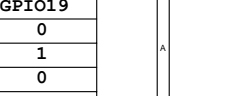
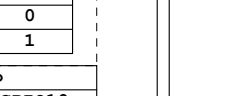
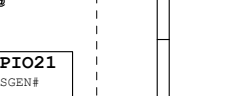
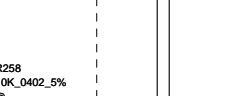
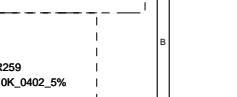
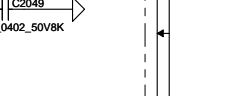
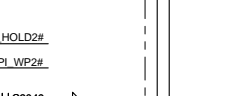
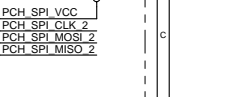
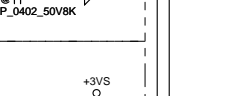
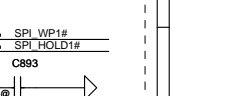
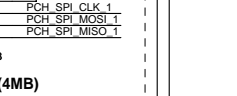
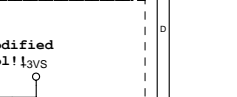
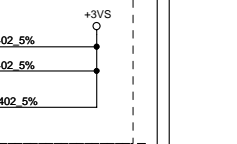
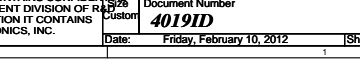
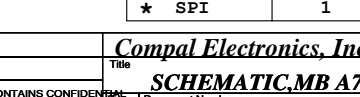
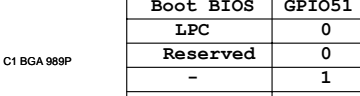
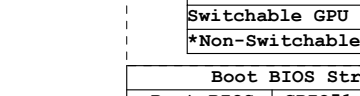
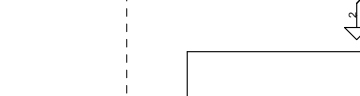
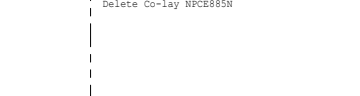
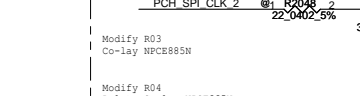
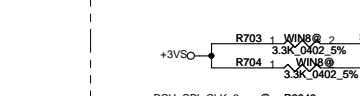
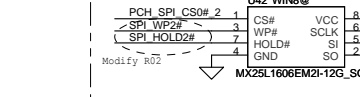
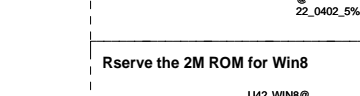
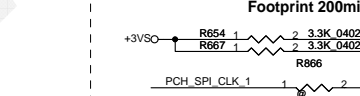
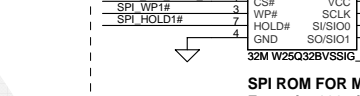
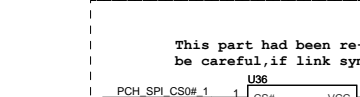
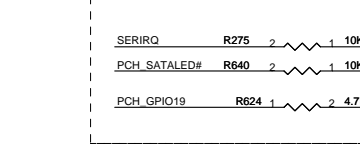
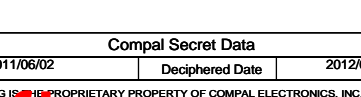
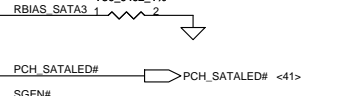
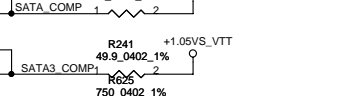
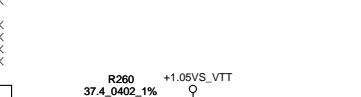
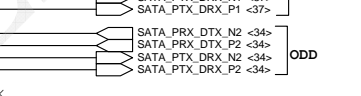
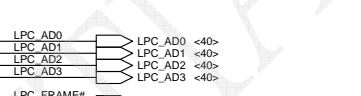
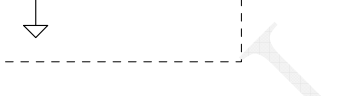
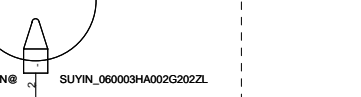
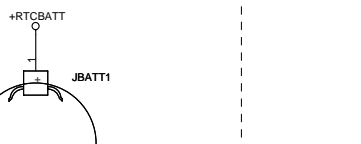
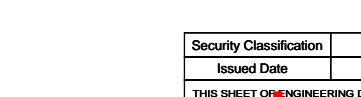
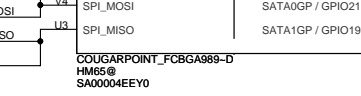
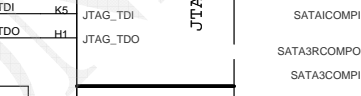
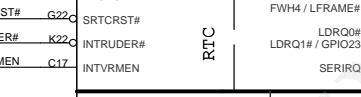
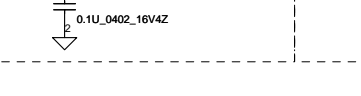
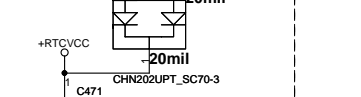
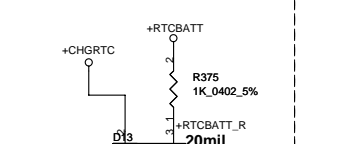
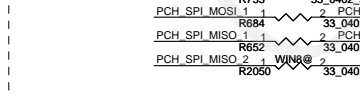
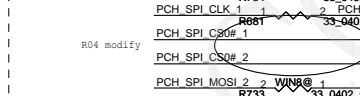
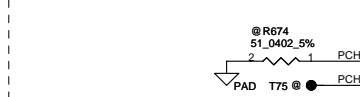
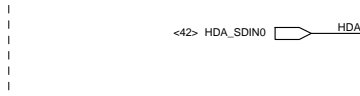
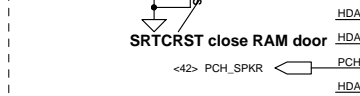
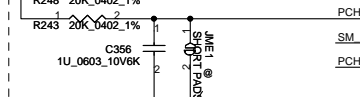
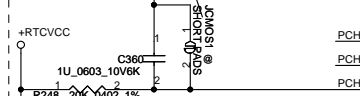
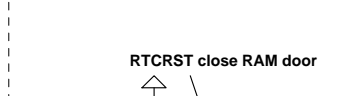
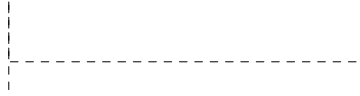
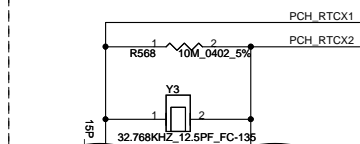
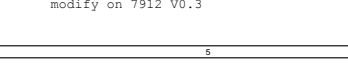
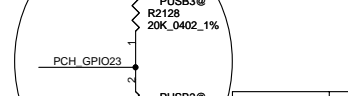
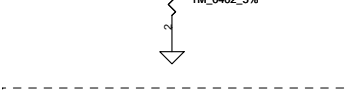
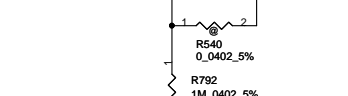
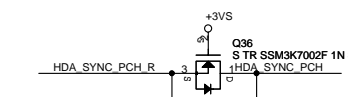
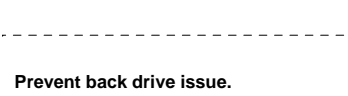
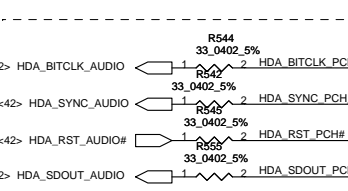
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)



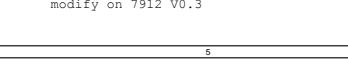
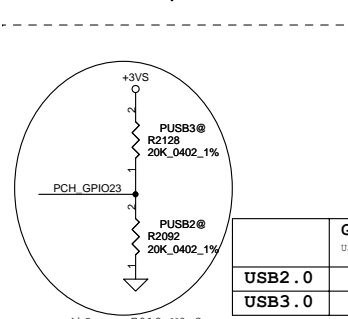
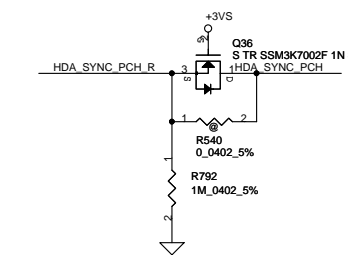
HDA_SDO as Capella ME override (GPIO33)
ME debug mode, this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]



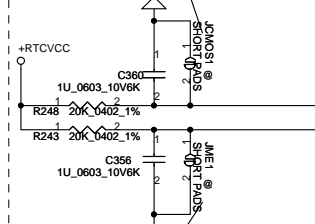
On Die PLL VR Select is supplied by
★ 1.5V when smaped high
1.8V when sampled low
Needs to be pulled High for Huron River platform



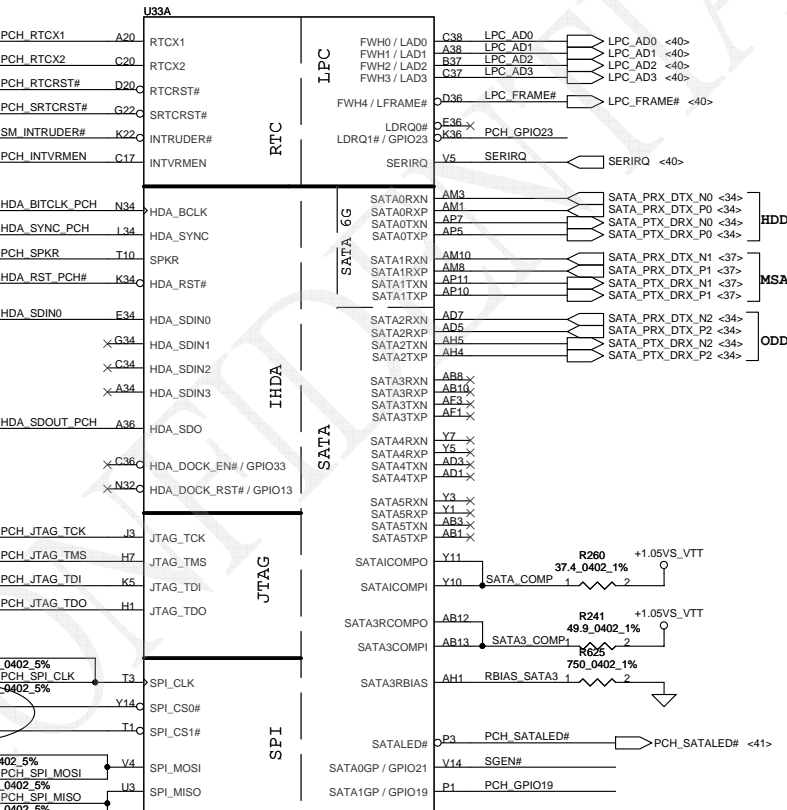
Prevent back drive issue.



RTCRST close RAM door



SRTCST close RAM door



modify on 7912 V0.3

www.vitalix.vn

RTCRST close RAM door

SRTCST close RAM door

RTCRST close RAM door

SRTCST close RAM door

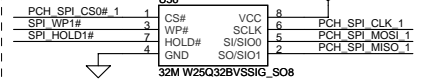
U33

B082HM77 QPRG C1 BGA 989P

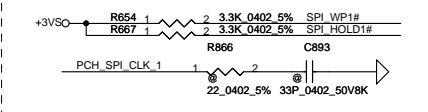
HM77@

SA00005AG00

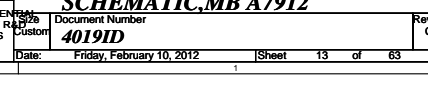
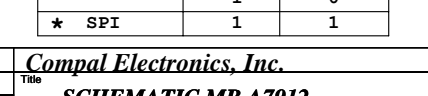
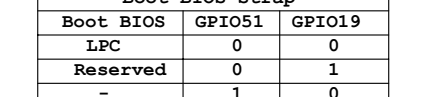
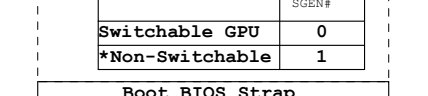
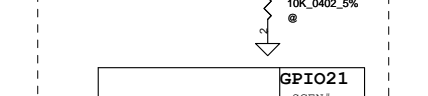
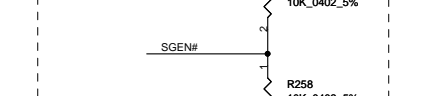
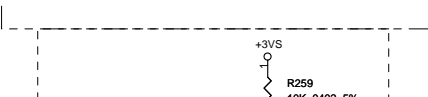
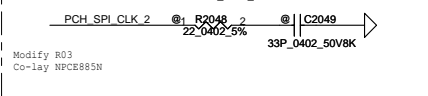
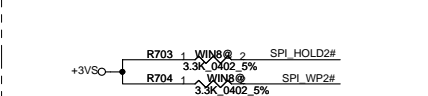
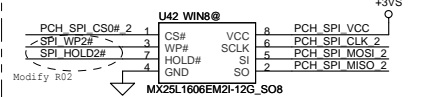
This part had been re-modified
be careful, if link symbol!!



SPI ROM FOR ME (4MB)
Footprint 200mil



Rserve the 2M ROM for Win8



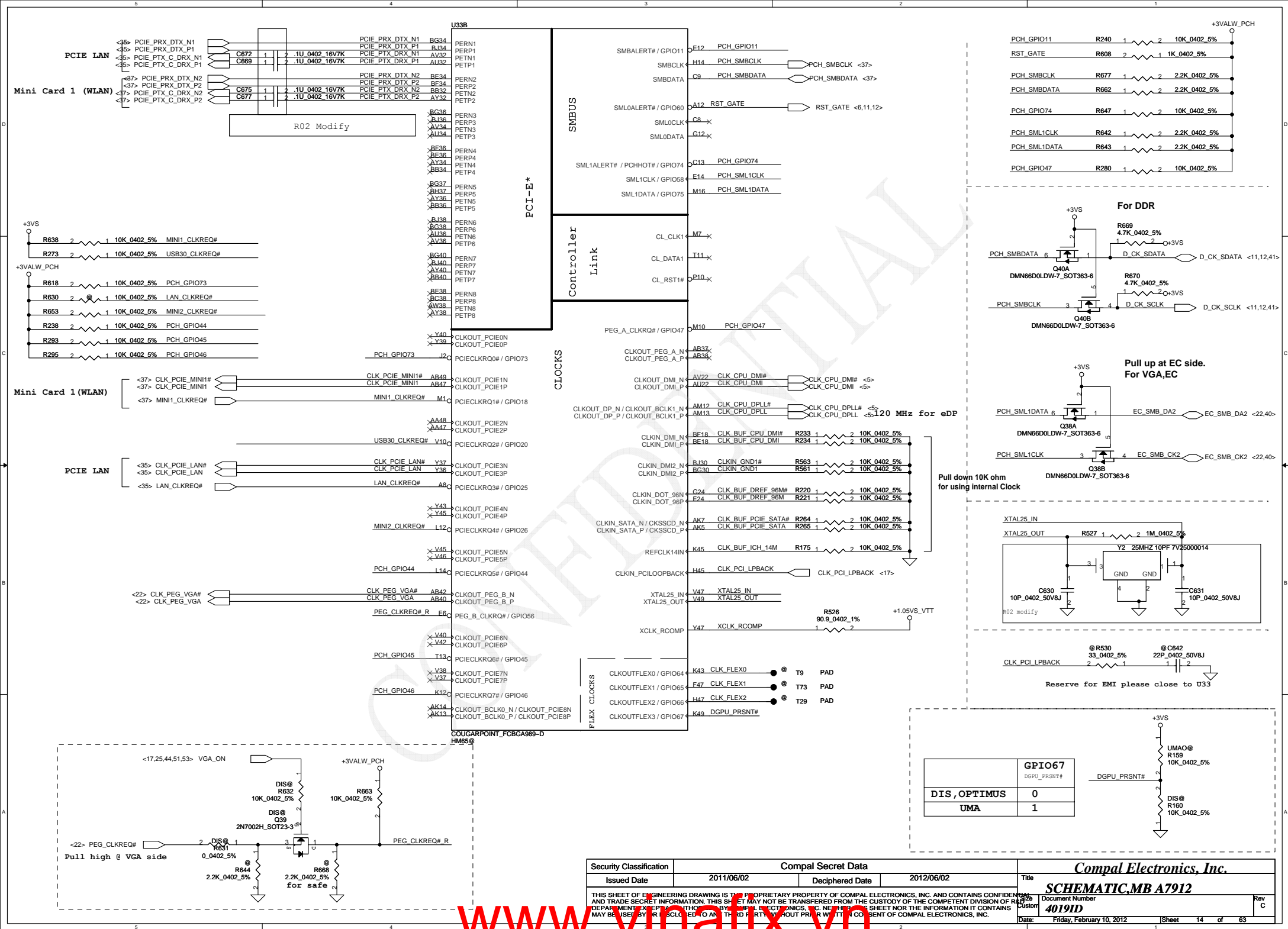
Security Classification	Compal Secret Data
Issued Date	2011/06/02
Deciphered Date	2012/06/02

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Compal Electronics, Inc.
Title
SCHEMATIC, MB A7912

Document Number
40191D

Date: Friday, February 10, 2012 Sheet 13 of 63



<40> ENBKL ENBKL R532 2 0.0402_5% IGPU_BKLT_EN

+3VS
R174 1 2.2K_0402_5% CTRL_CLK
R158 1 2.2K_0402_5% CTRL_DATA
R156 1 2.2K_0402_5% PCH_LCD_CLK
R157 1 2.2K_0402_5% PCH_LCD_DATA

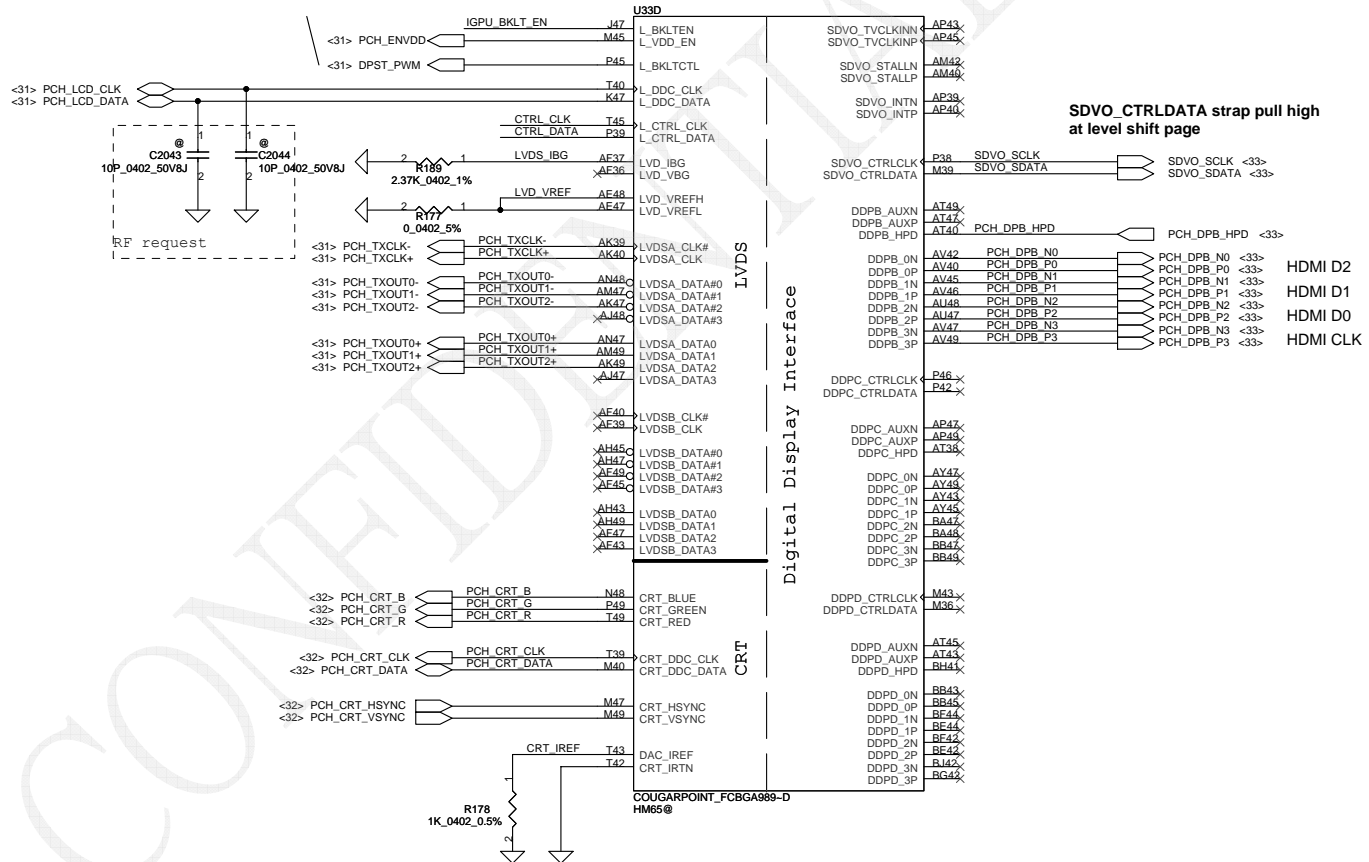
+3VS
R521 1 2.2K_0402_5% PCH_CRT_CLK
R522 1 2.2K_0402_5% PCH_CRT_DATA

R534 1 2.150_0402_1% PCH_CRT_B
R533 1 2.150_0402_1% PCH_CRT_G
R535 1 2.150_0402_1% PCH_CRT_R

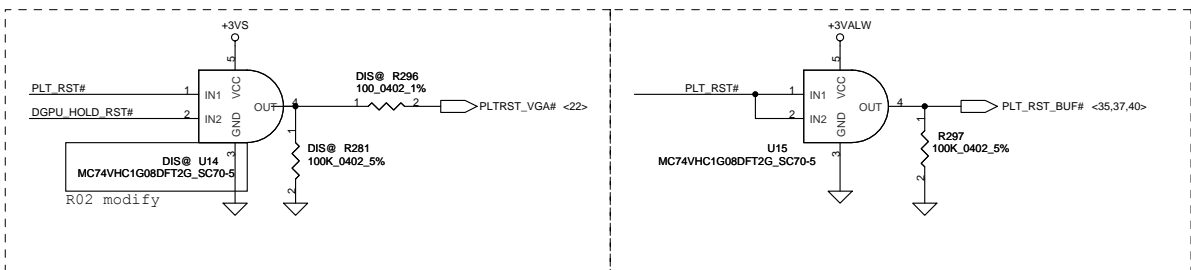
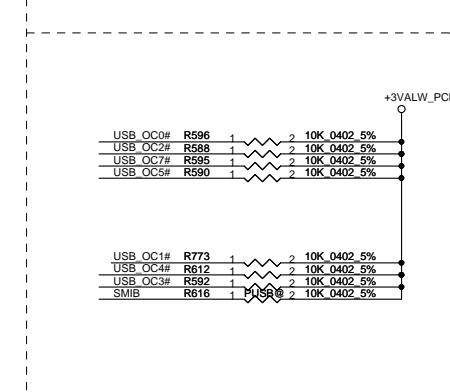
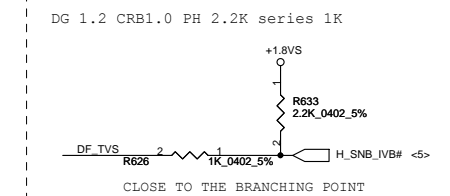
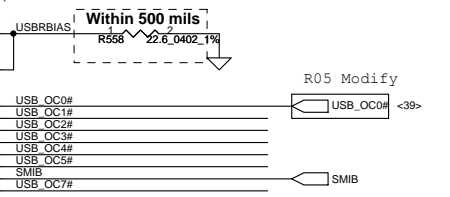
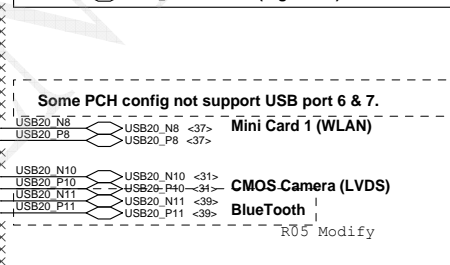
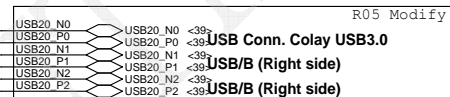
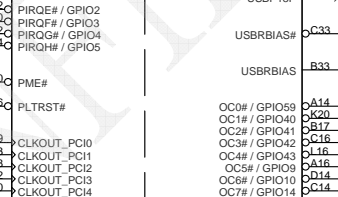
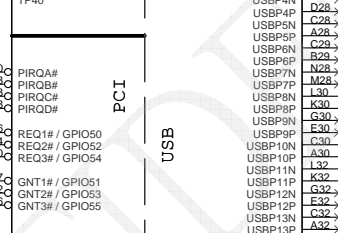
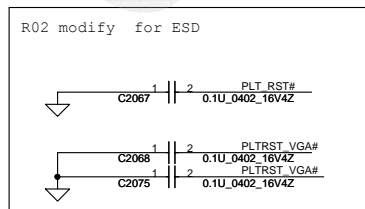
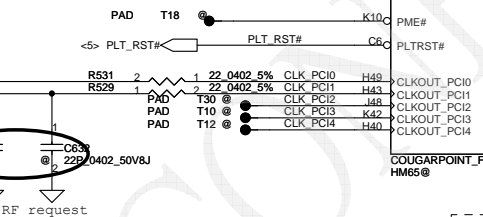
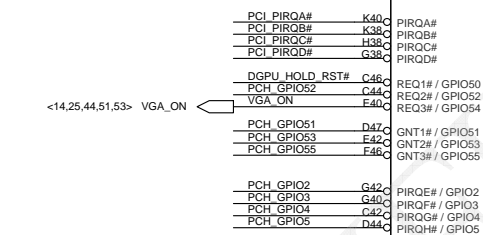
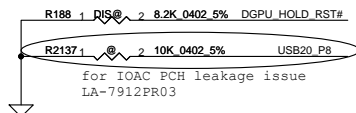
R02 Modify

C2076 1 1U_0402_6.3V6K PCH_DPB_HPD

Pull high at LVDS conn side.



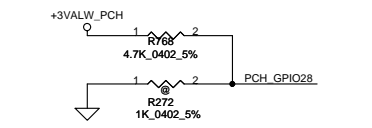
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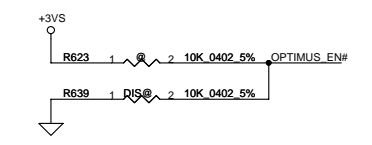
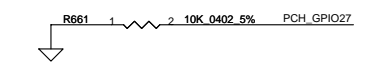
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HDA_SYNC PH(PLL =+1.5VS)
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

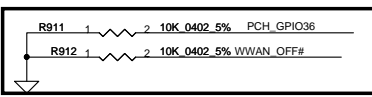
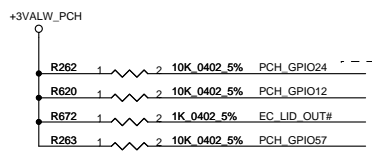


Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70



	GPIO38 OPTIMUS_EN#
★ OPTIMUS	0
DIS Only	1

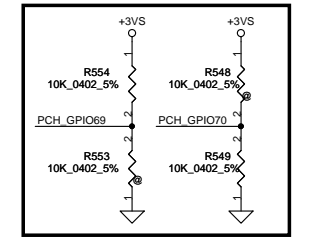
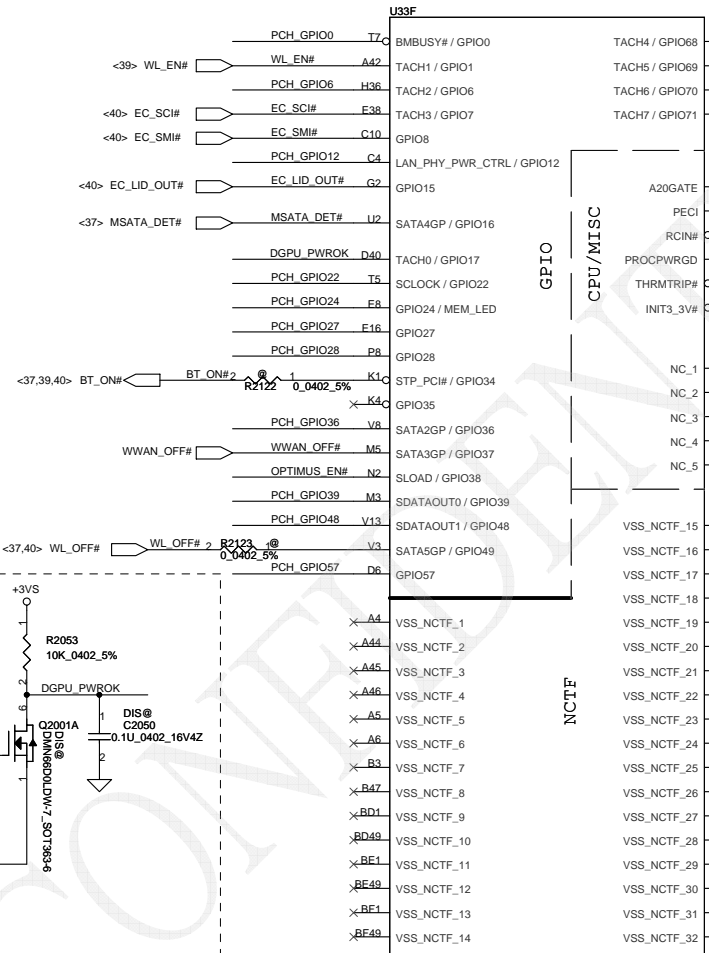
R277	1	2	200K_0402_5%	WWAN_OFF#
R276	1	2	10K_0402_5%	PCH_GPIO0
R546	1	2	10K_0402_5%	WL_EN#
R191	1	2	10K_0402_5%	PCH_GPIO6
R641	1	2	10K_0402_5%	MSATA_DET#
R290	1	2	10K_0402_5%	PCH_GPIO22
R649	1	2	10K_0402_5%	PCH_GPIO39
R291	1	2	200K_0402_5%	PCH_GPIO36
R619	1	2	10K_0402_5%	BT_ON#
R292	1	2	10K_0402_5%	PCH_GPIO48
R274	1	2	10K_0402_5%	WL_OFF#



GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

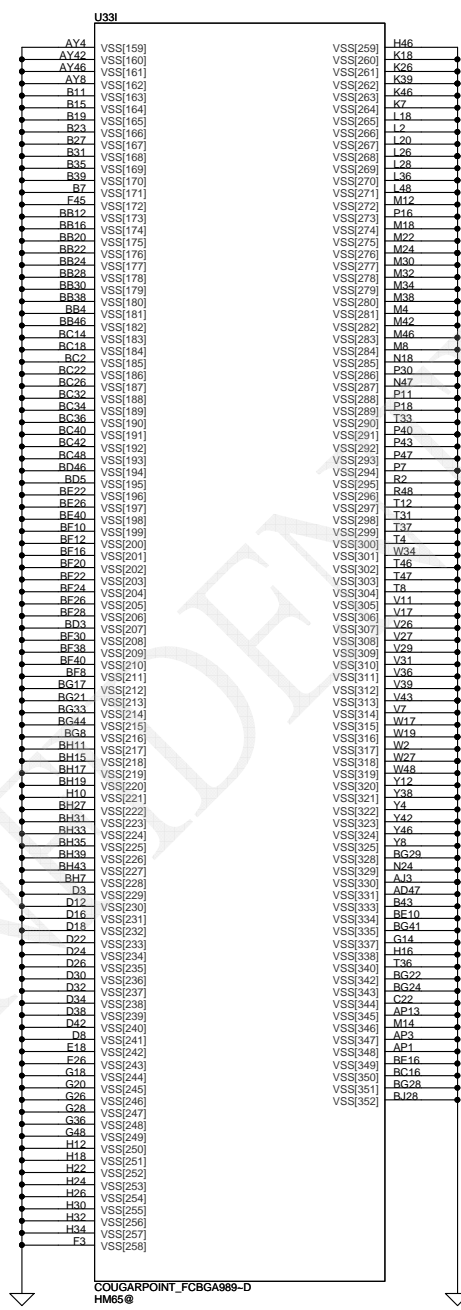
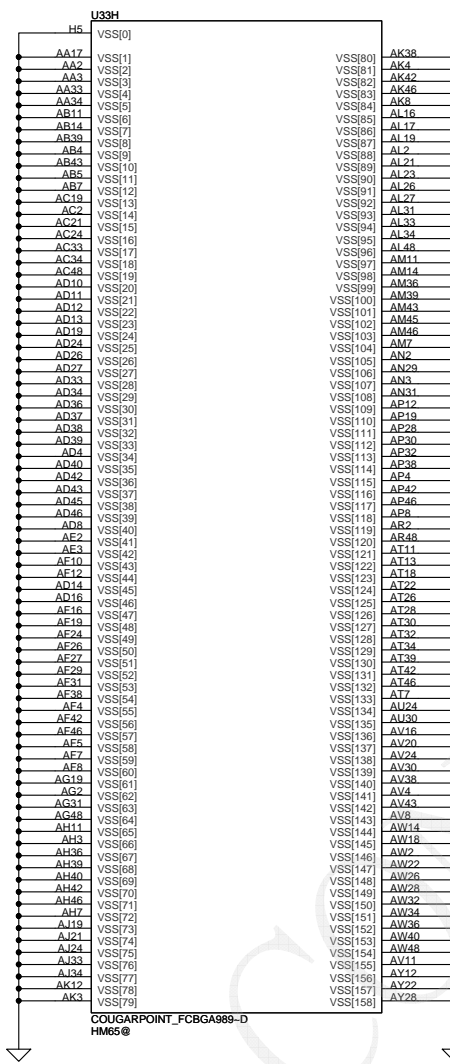
CRB1.0 PH10K to +3VALW

GPIO36/GPIO37 is Strap functionality that requires internal pull down to be sampled at rising PWROK. When uses as SATA2GP/SATA3GP for mechanical presence detect - use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input - ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP - use 8.2K-10K pull-down
check list page 47

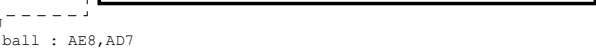
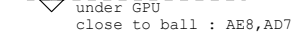
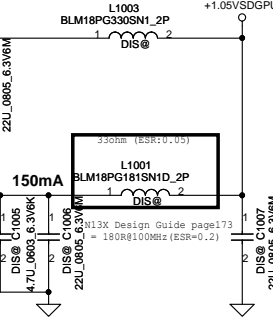


Project ID	GPIO69	GPIO70
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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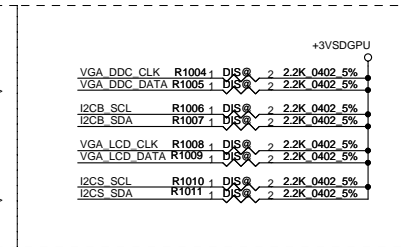
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U1001

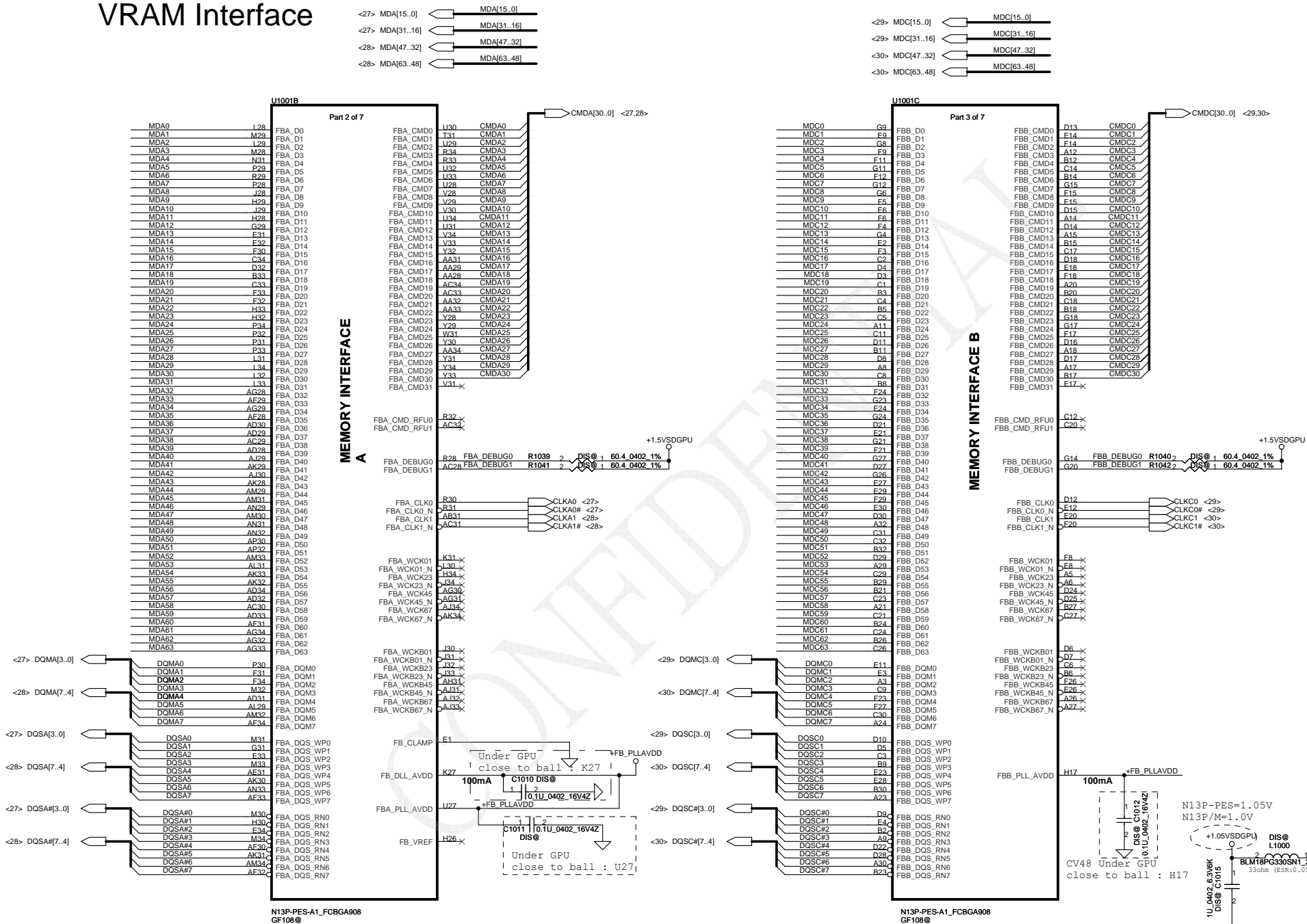


N13M-GS FCBGA 908P
GM@
SA000057E20



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VRAM Interface



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+3VSDGPU for GPU

The schematic diagram illustrates the +3VSDGPU for GPU circuit. Key components and connections include:

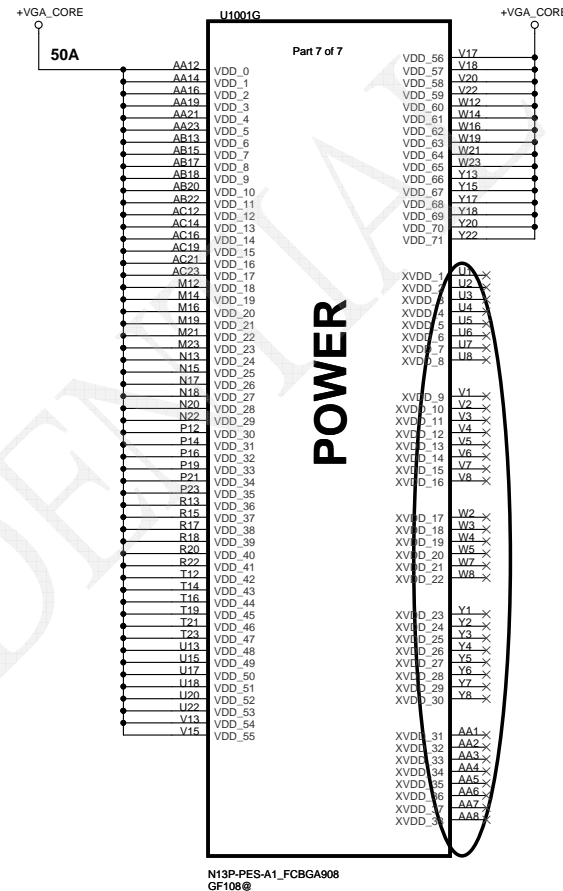
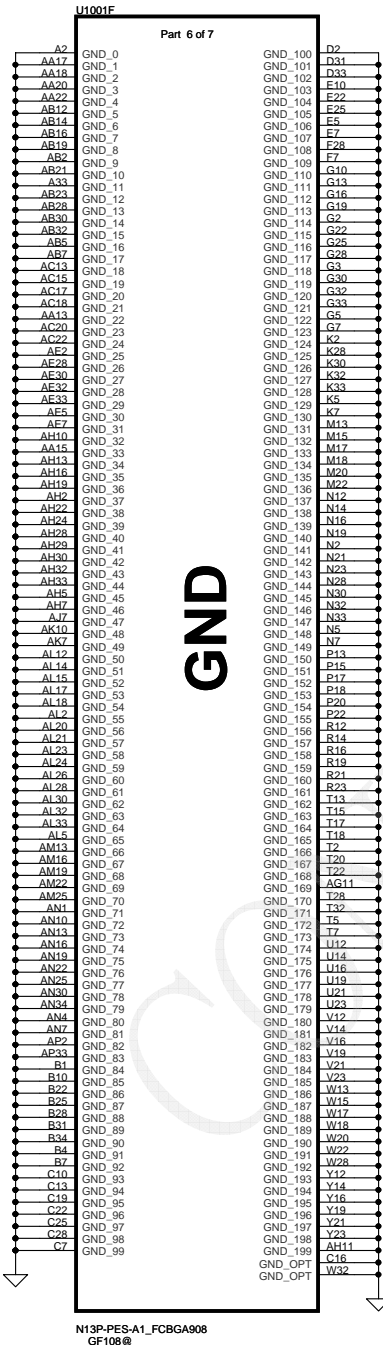
- Inputs:** +3VSDGPU, +3VALW, +3V, and a signal from the VGA_ON pin (<14,17,44,51,53>).
- Resistors:** R514 (1K_0402_5%), R515 (100K_0402_5%), R519 (4.7K_0402_5%), and R511 (470_0603_5%).
- Capacitors:** C603 (0.1u_0603_25V7K), C602 (4.7u_0603_6.3V6K), C612 (0.1u_0603_25V7K), and C609 (4.7u_0603_6.3V6K).
- Transistors:** Q35A (DMN66D0LDW-7_SOT363-6), Q33 (AP2301GN-HF_SOT23-3), and Q35B (DMN66D0LDW-7_SOT363-6).
- Logic Gates:** 3VSDelay_gate and 43VSDelay_gate.
- Other Components:** A 100mil(1.5A) current source and a 3VSDelay gate.
- Notes:** "Modify R03" is indicated near the R519 component.

POWER

Design guide no define

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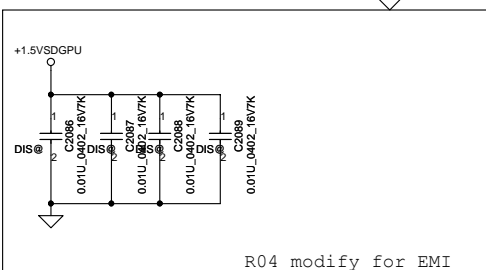
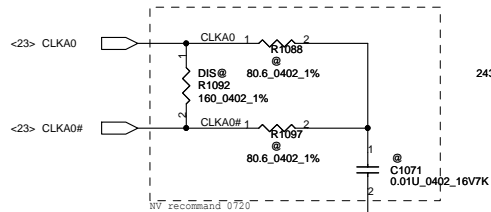
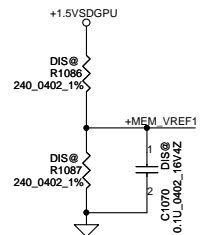
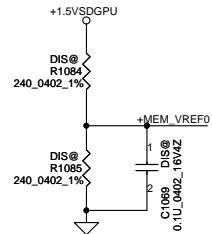


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VRAM DDR3 chips (1GB)

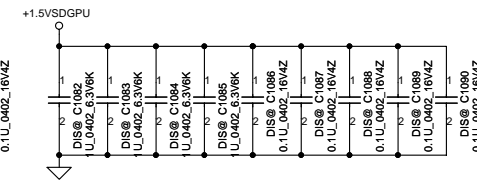
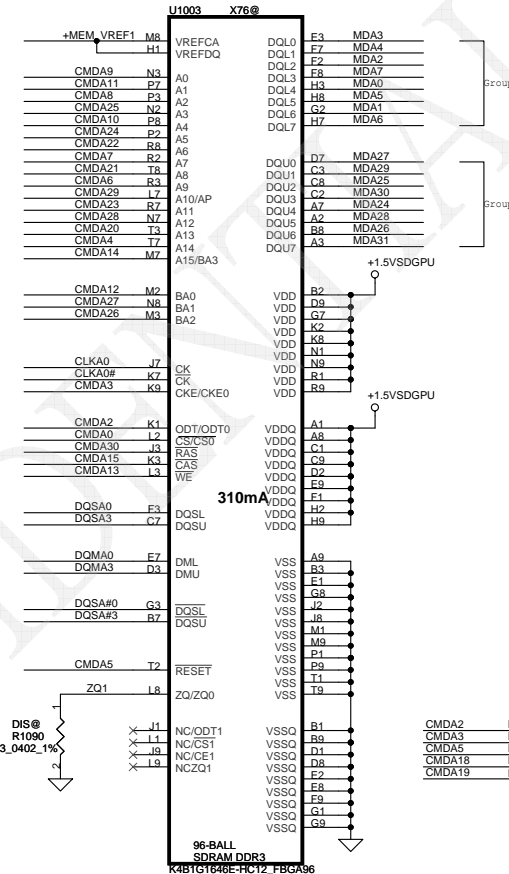
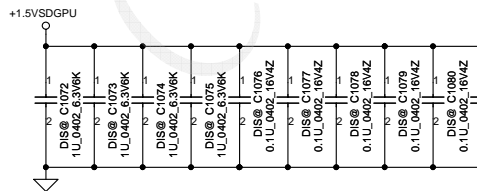
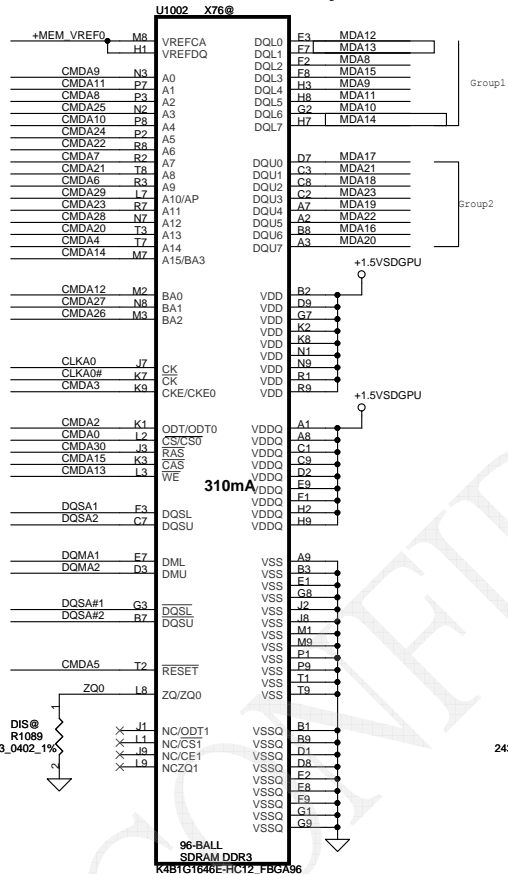
64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

<23,28> DQSA[7..0] DQSA[7..0]
<23,28> DQSA#7..0 DQSA#7..0
<23,28> DQMA[7..0] DQMA[7..0]
<23,28> MDA[63..0] MDA[63..0]
<23,28> CMDA[30..0] CMDA[30..0]



R04 modify for EMI

R02 modify
Swap MDA13 and MDA14



CMDA2 R1091 DIS@ 2 10K 0402 5%
CMDA3 R1093 DIS@ 2 10K 0402 5%
CMDA5 R1094 DIS@ 2 10K 0402 5%
CMDA18 R1095 DIS@ 2 10K 0402 5%
CMDA19 R1096 DIS@ 2 10K 0402 5%

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CAS*	No Termination

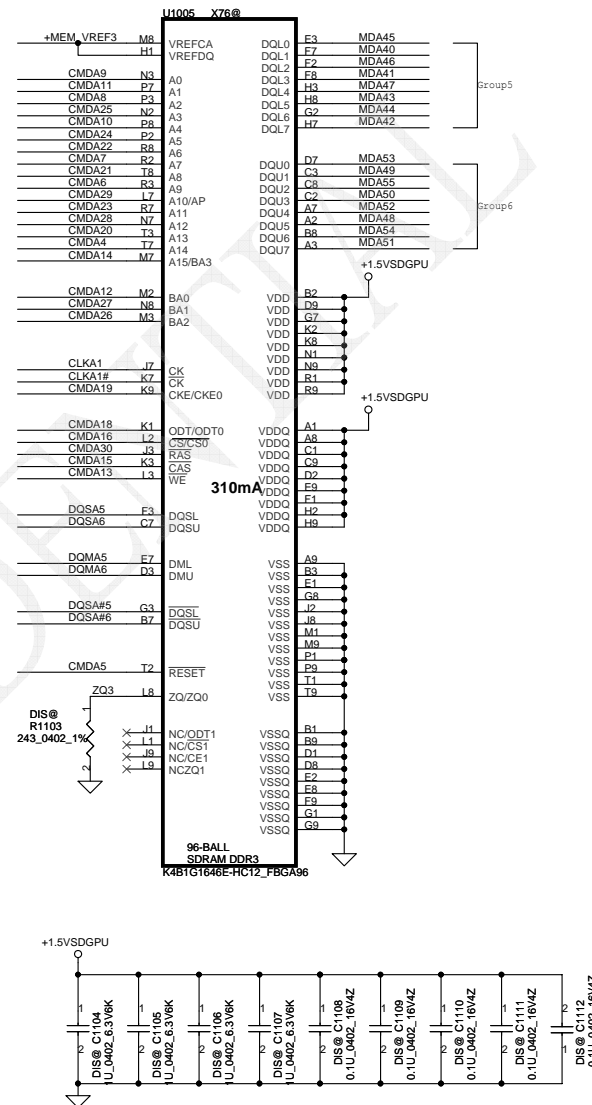
Hynix : SA00003YO20 (S IC D3 128M16 H5TQ2G63BFR-11C FBGA)
Hynix : SA000041S40 (S IC D3 64Mx16 H5TQ1G63DFR-11C FBGA)

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

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128Mx16 DDR3 *8==>2GB

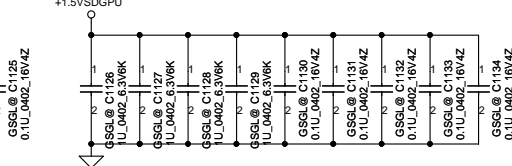
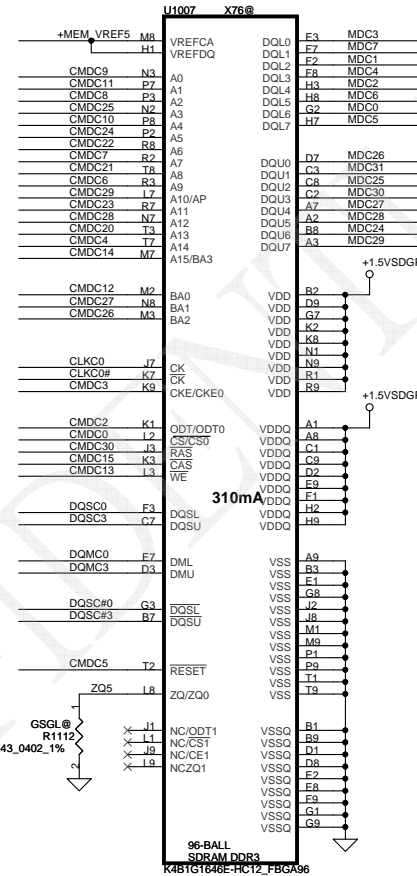
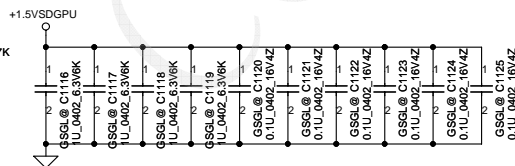
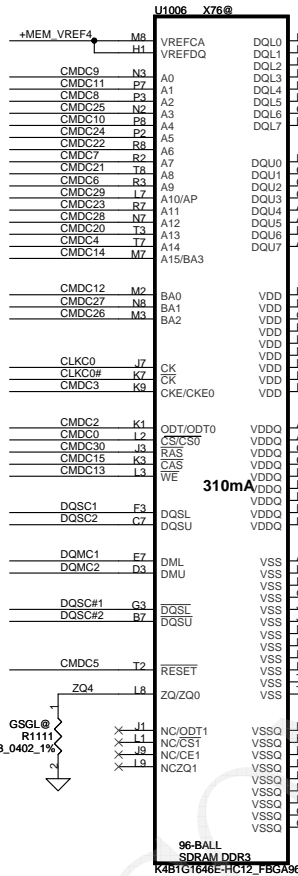
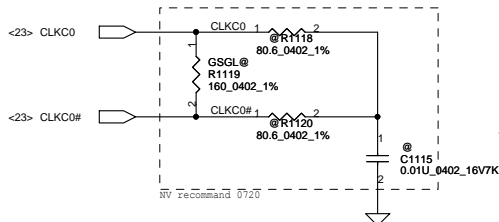
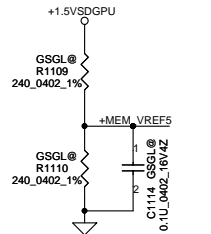
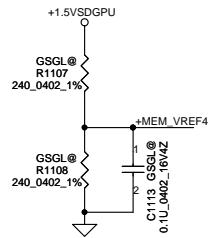
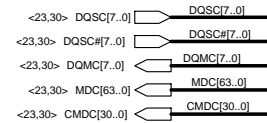


LOW HIGH

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

Command Bit	Default Pull-down
ODT#	10k
CKE#	10k
RST	10k
CS*	No Termination

CMDC2 R1113 GSGL @ 2 10K 0402 5%

CMDC3 R1114 GSGL @ 2 10K 0402 5%

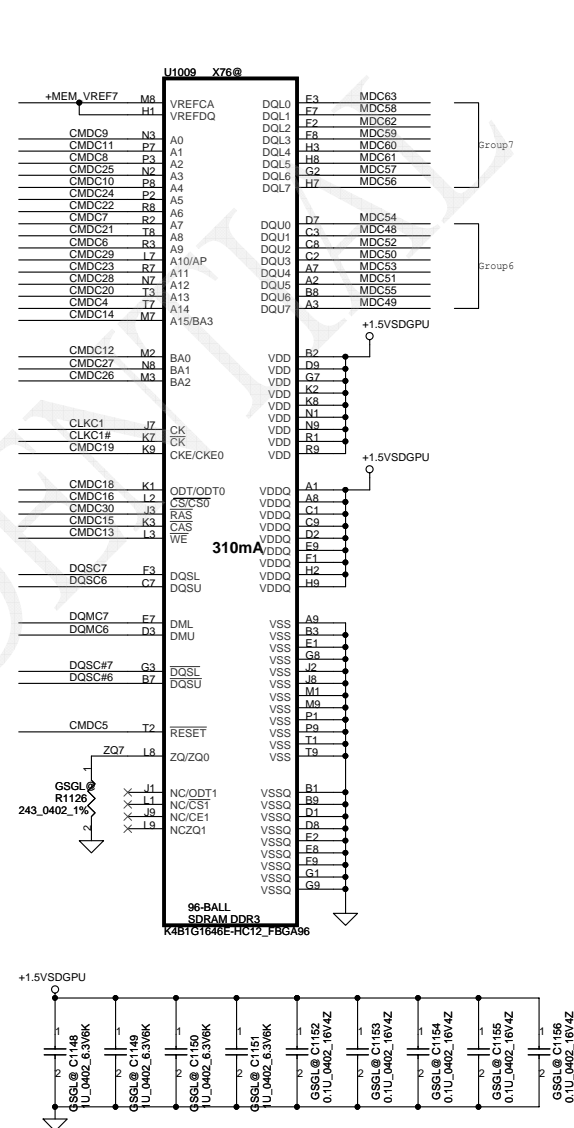
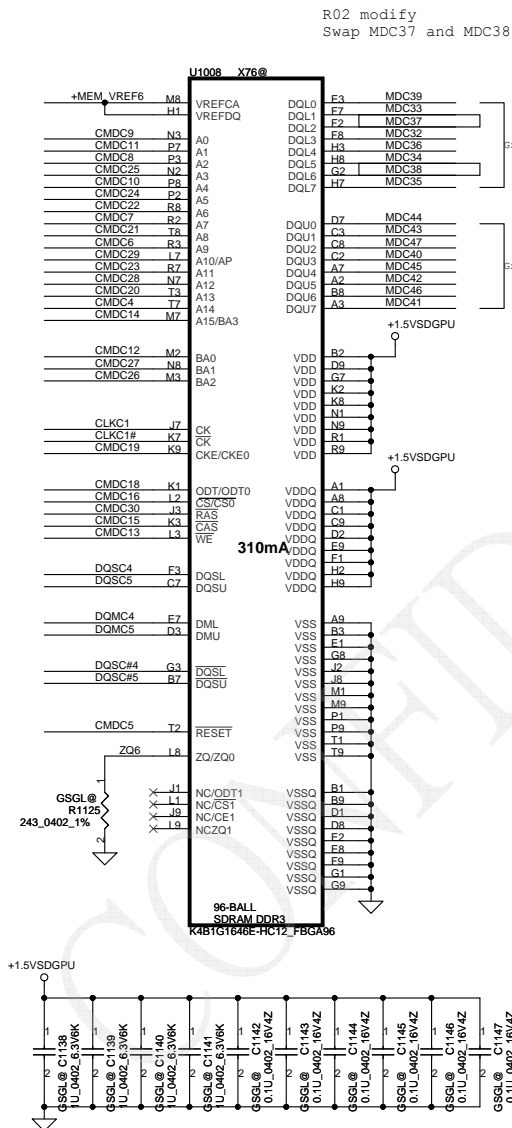
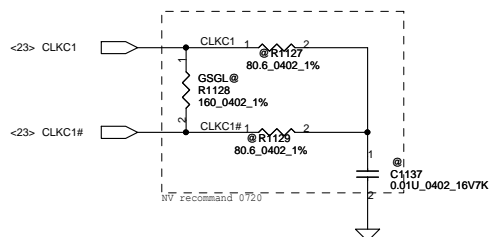
CMDC5 R1115 GSGL @ 2 10K 0402 5%

CMDC18 R1116 GSGL @ 2 10K 0402 5%

CMDC19 R1117 GSGL @ 2 10K 0402 5%

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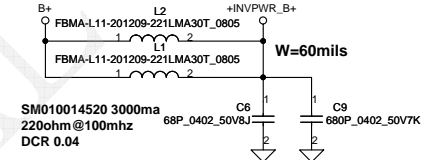
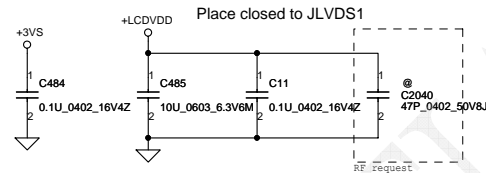
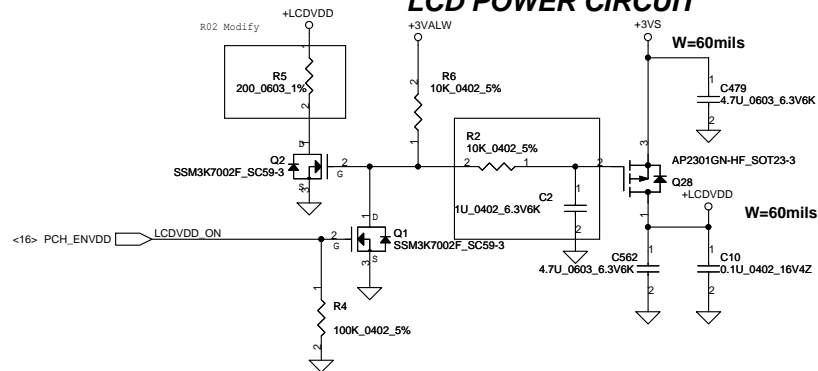
128Mx16 DDR3 *8==>2GB



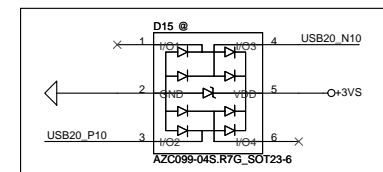
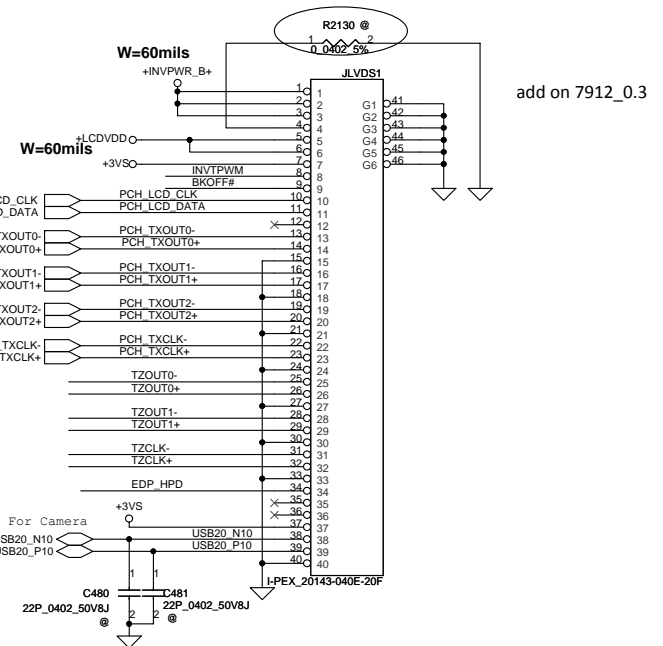
Mode D Address	0...31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

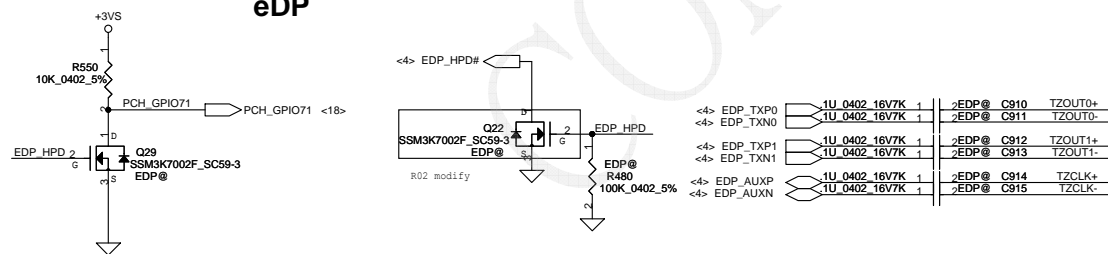
LCD POWER CIRCUIT



LCD/LED PANEL Conn.



eDP

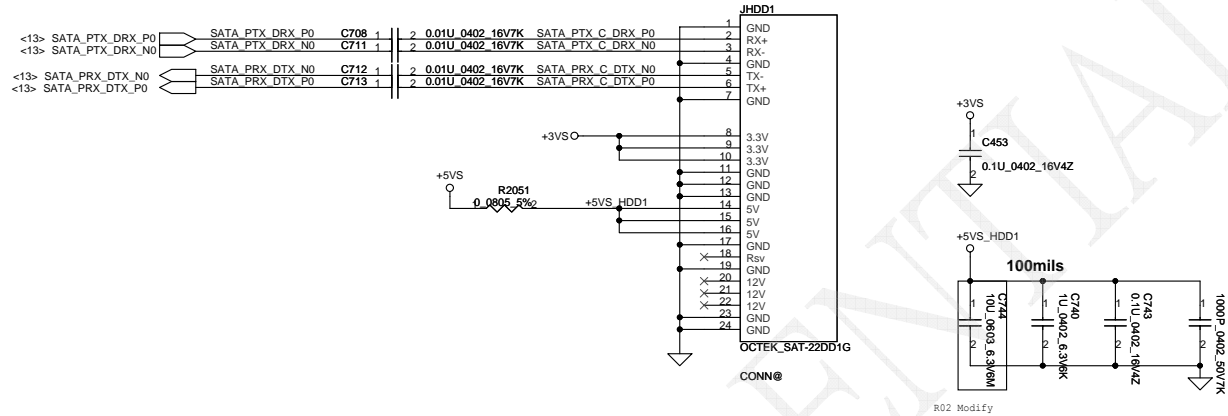


	GPIO71 PCH_GPIO71
eDP	0
LVDS	1

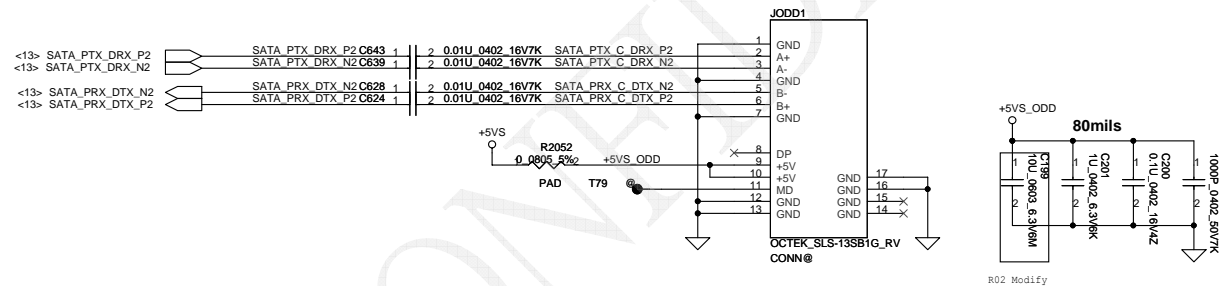
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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								4019ID			
Date: Friday, February 10, 2012								Sheet 31 of 63			

SATA HDD1 Conn.

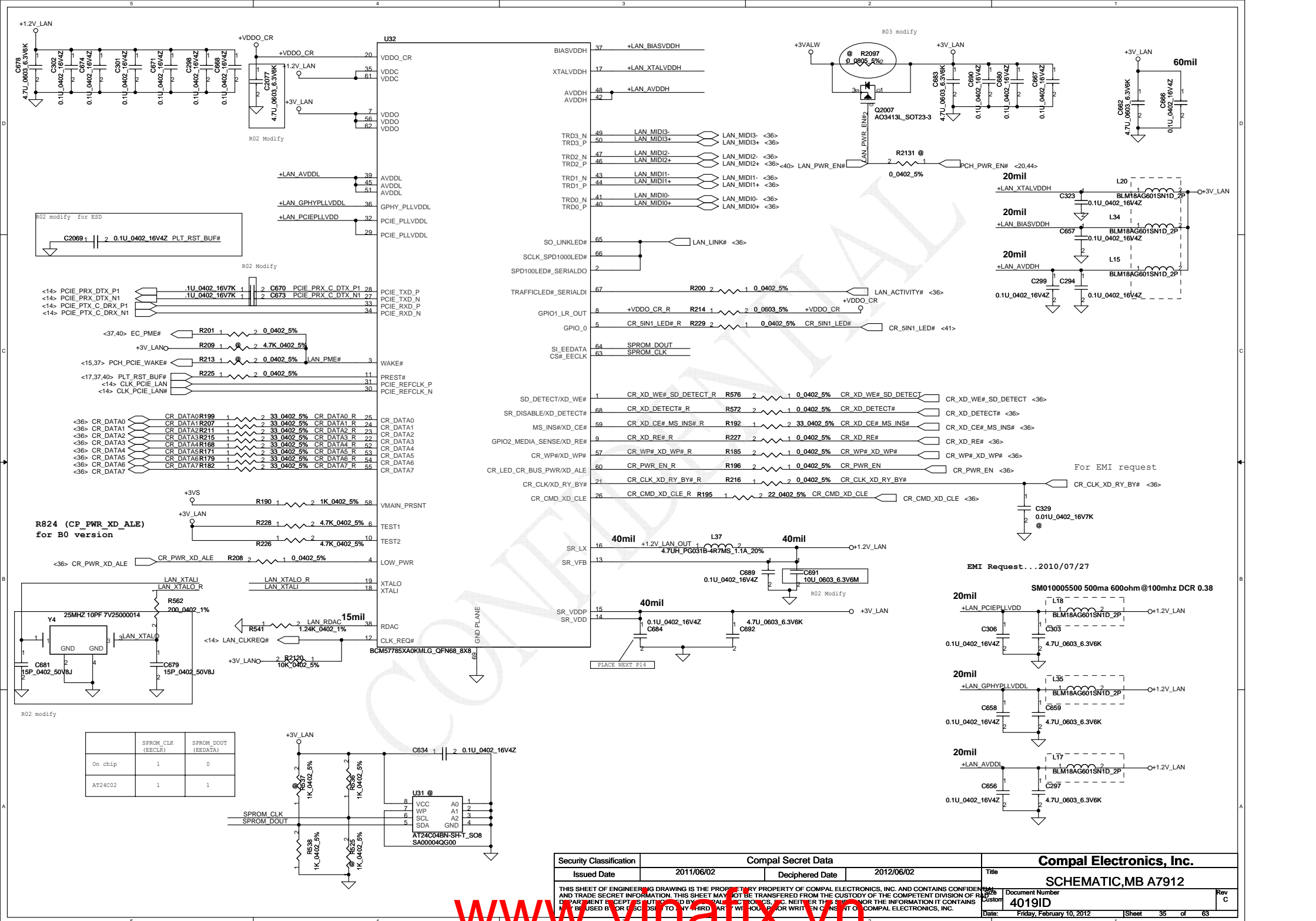
CL 4.0 mm



SATA ODD Conn.

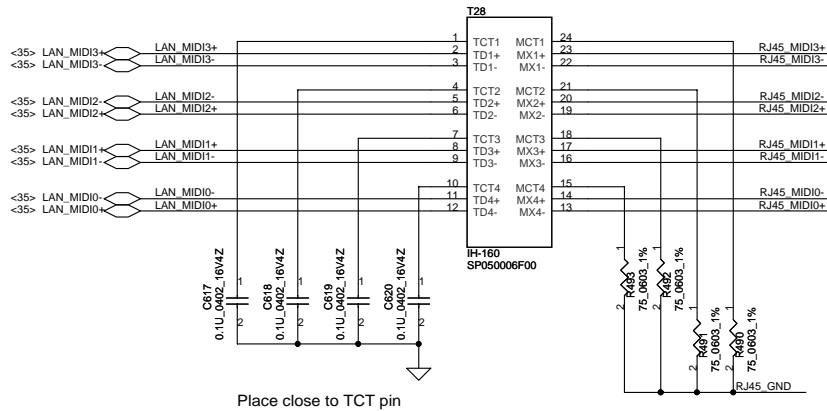


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				Date:	Friday, February 10, 2012	Sheet	34 of 63

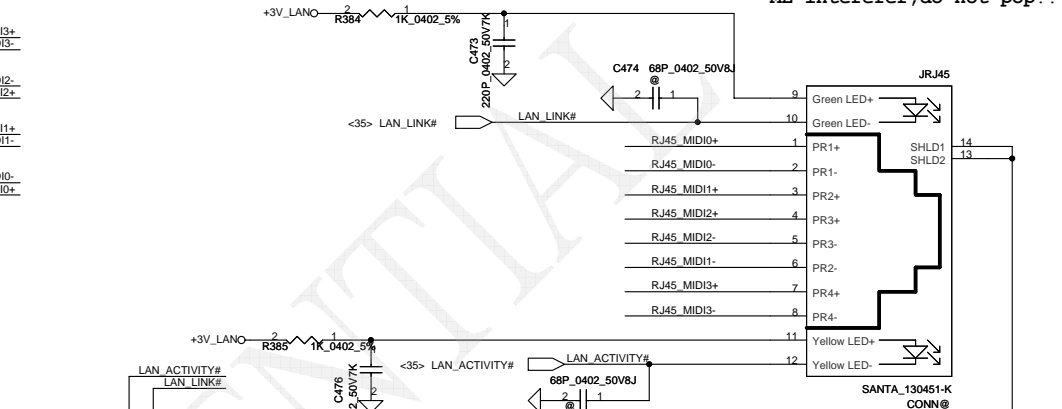


LAN Connector

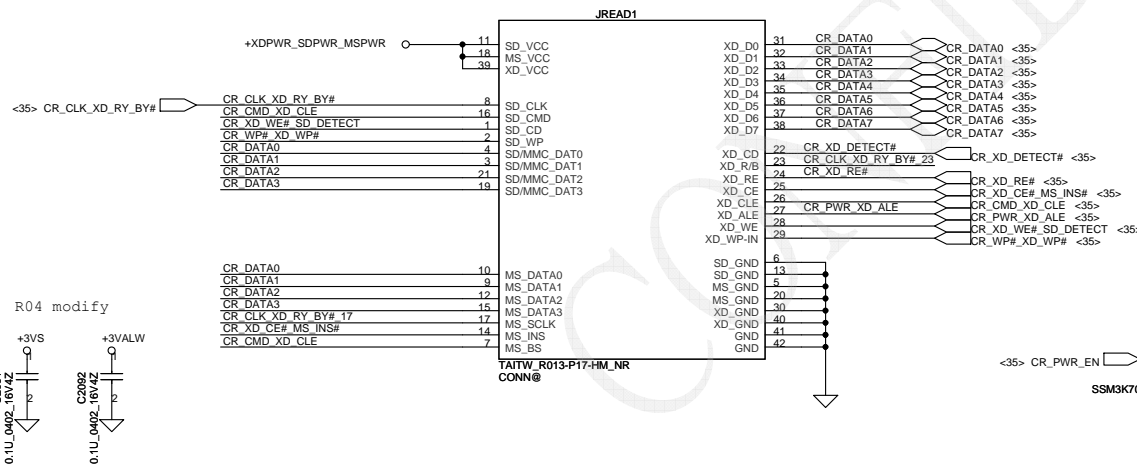
C474, C475 and D14
ME interfere, do not pop!!



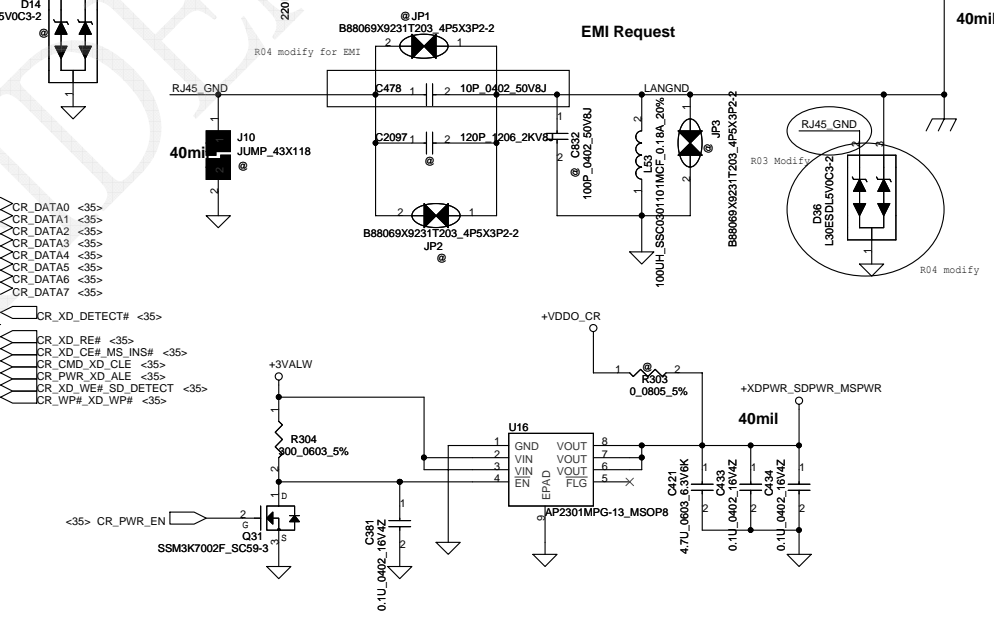
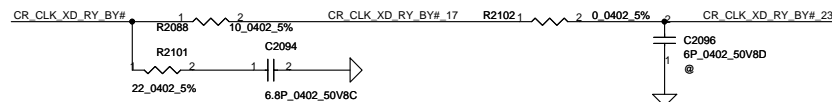
BOTH HAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG: S X'FORM_ IH-160 LAN, SP050006F00



Card Reader Connector

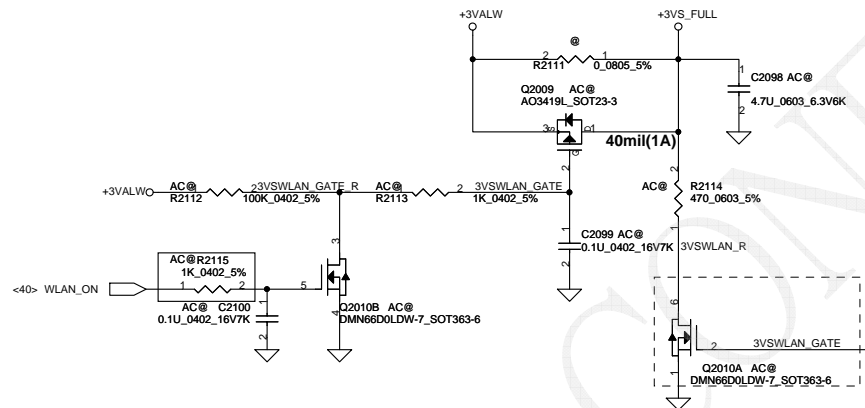
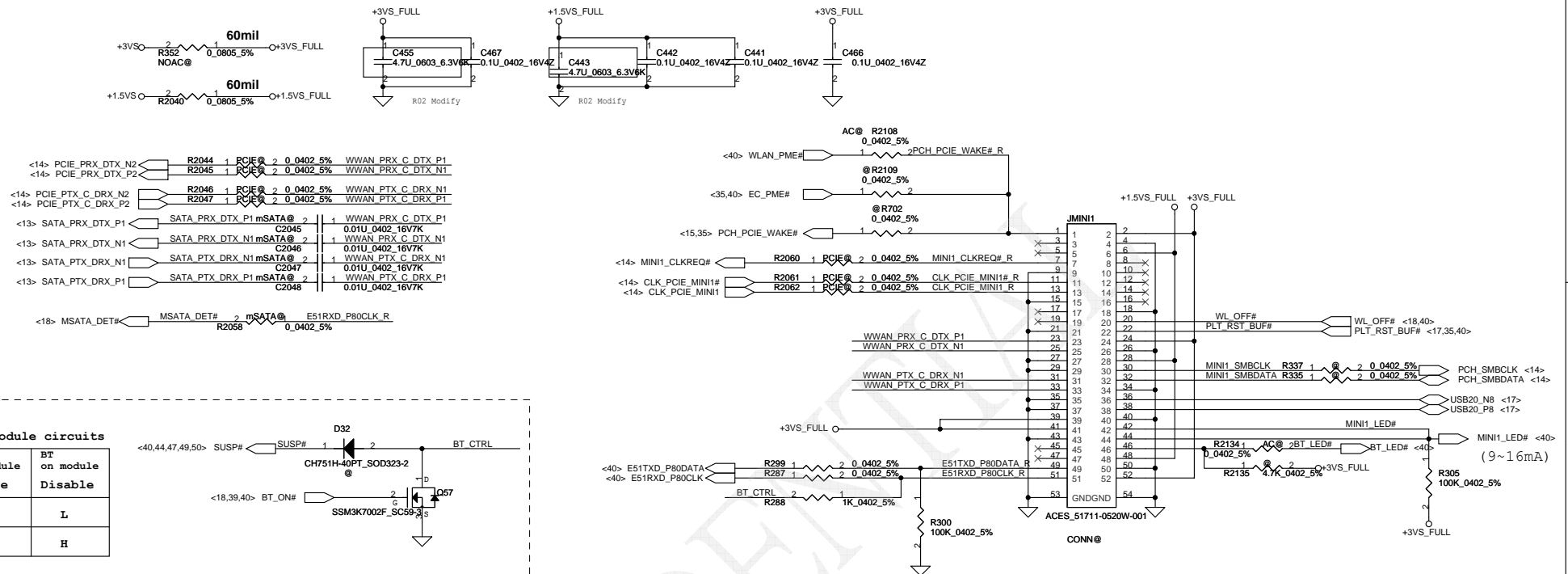


R02 modify for SD3.0 issue



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For Wireless LAN or MSATA



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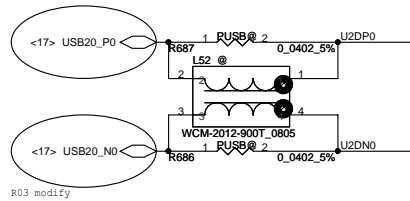
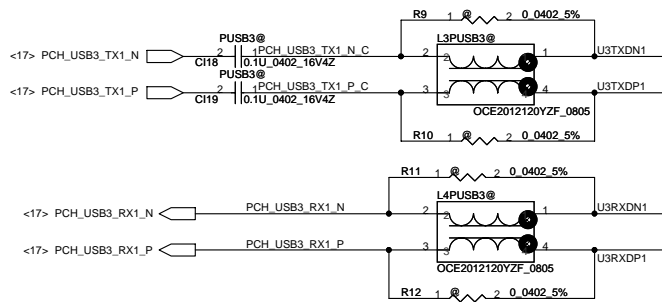
CONFIDENTIAL

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				40191D	
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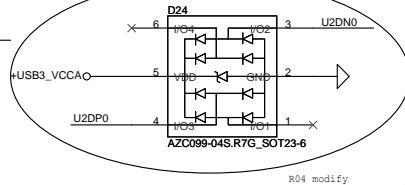
Default use PCH side USB3.0 signal

For USB2.0 ESD request

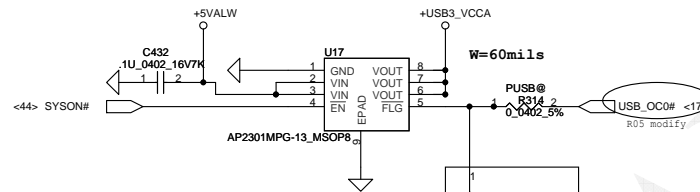
Default use PCH side USB3.0 signal



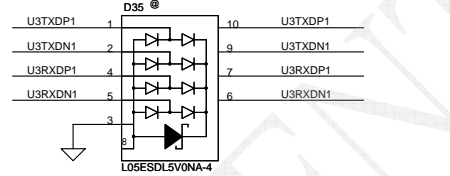
For USB2.0 ESD request



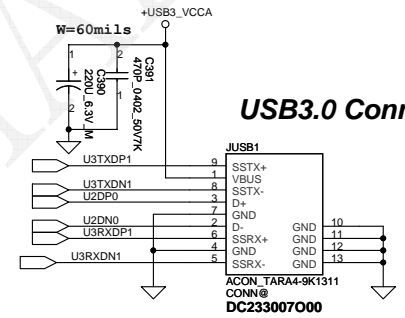
R04 modify



For ESD request



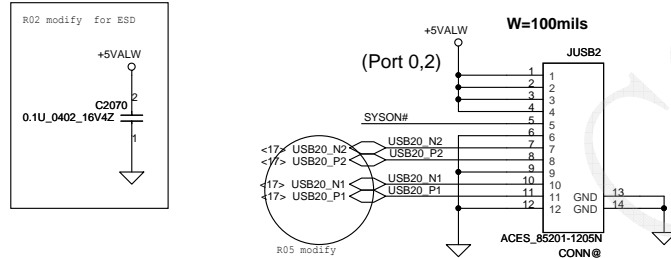
U3TXDN1
U3TXDN1
U3RXDN1
U2DN0
U3RXDN1
U3RXDN1



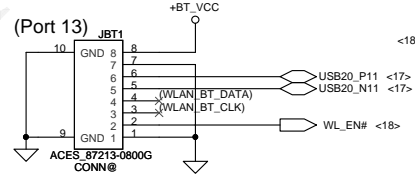
USB3.0 Conn.

USB/B Conn.

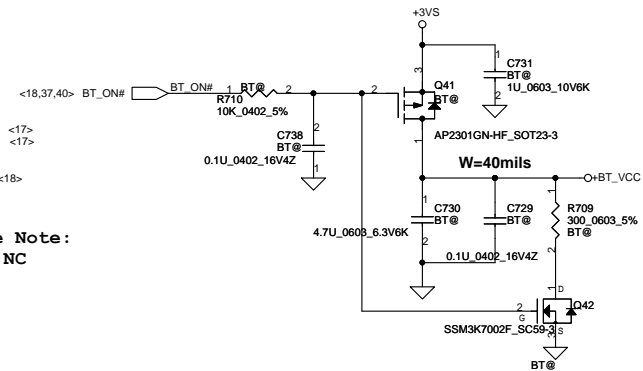
BT Conn.



R05 modify

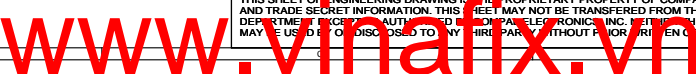


BT Wire Cable Note:
Pin 3, Pin 4 NC

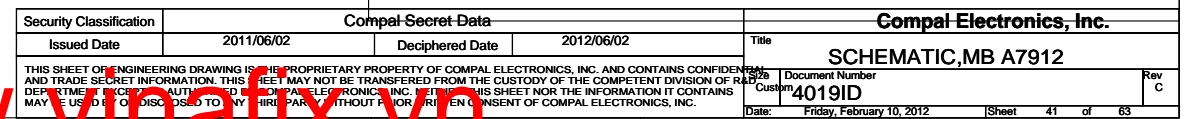
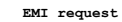
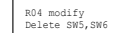


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MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Date	Friday, February 10, 2012
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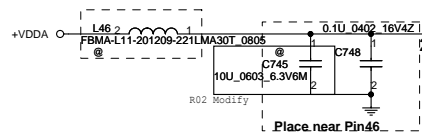
www.vinallix.vn



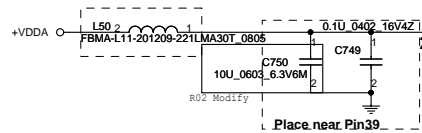
Test Only
Bottom Side



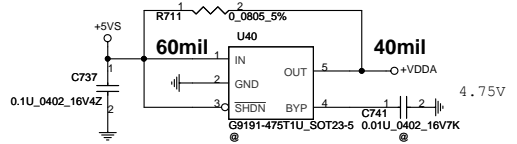
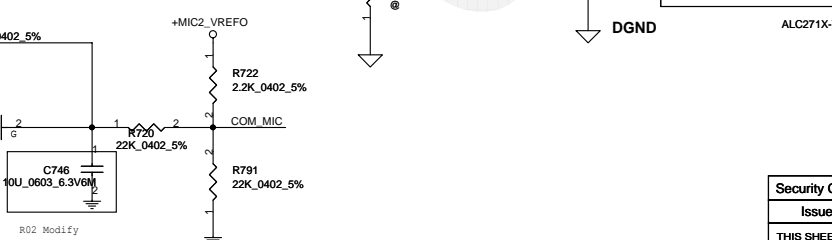
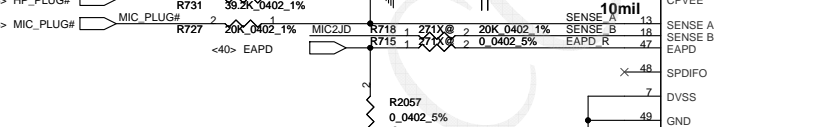
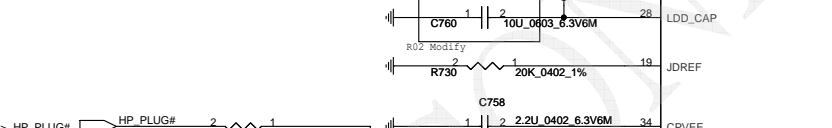
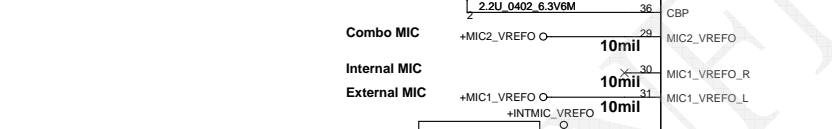
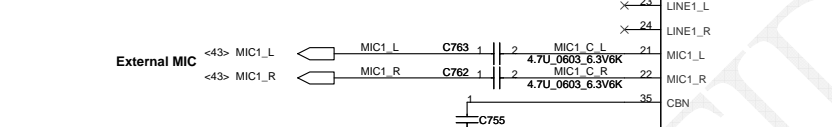
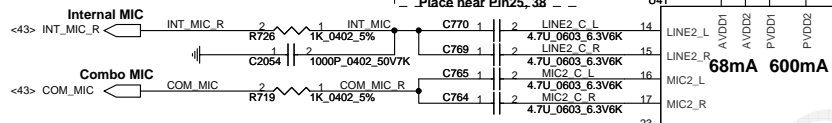
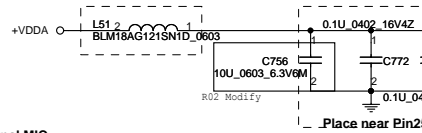
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04

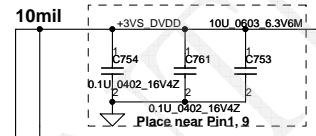


SM010030010 200ma 120ohm@100mhz DCR 0.2

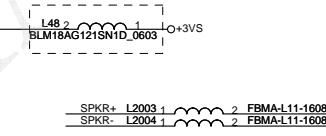


(output = 300 mA)

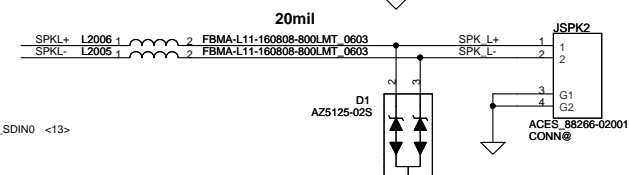
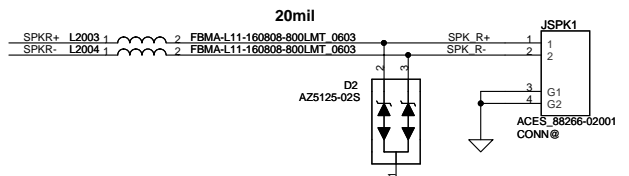
HD Audio Codec



SM010030010 200ma 120ohm@100mhz DCR 0.2

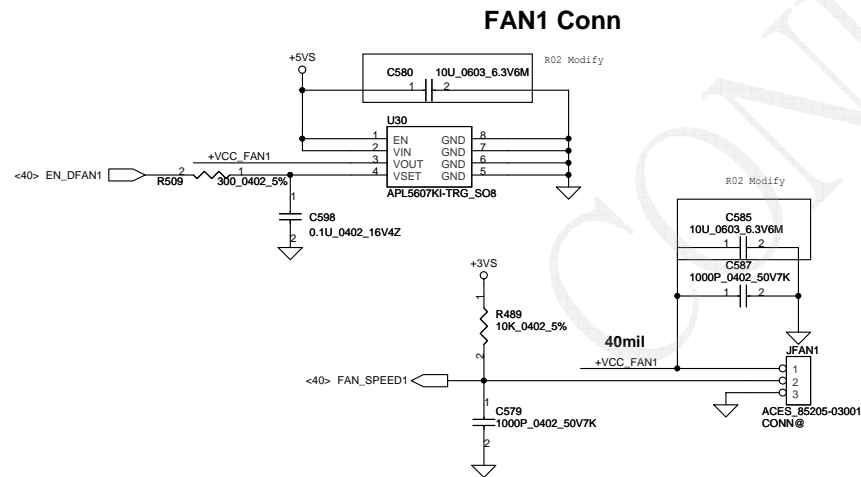
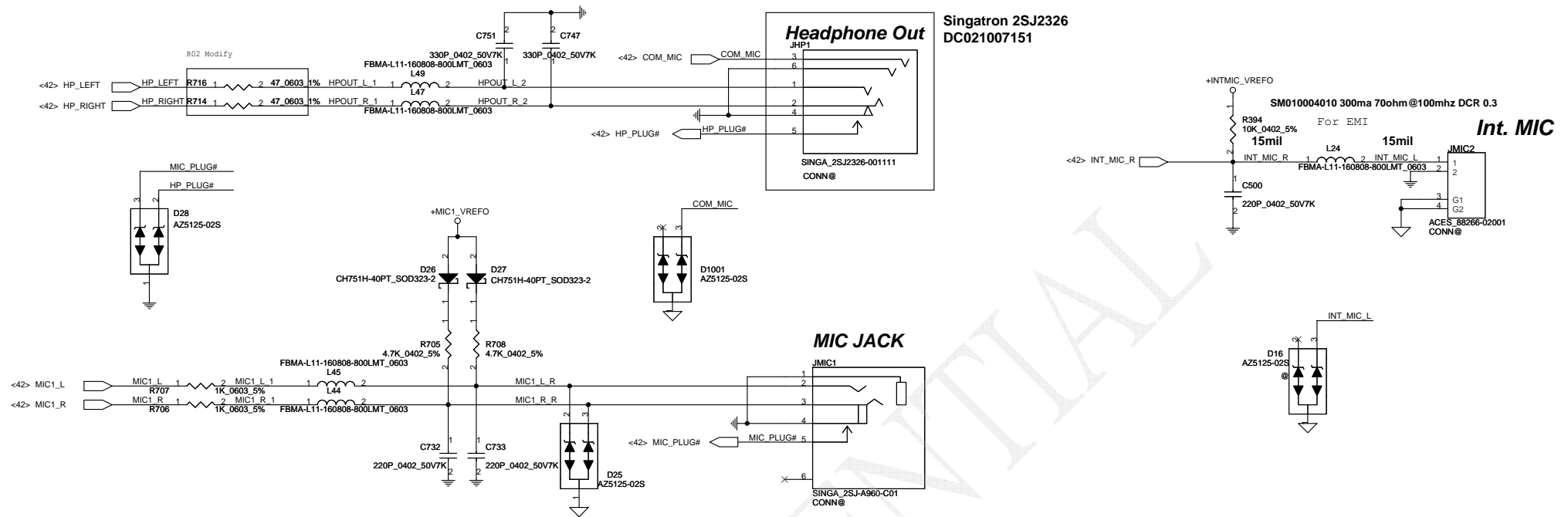


Int. Speaker Conn.

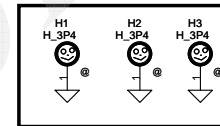


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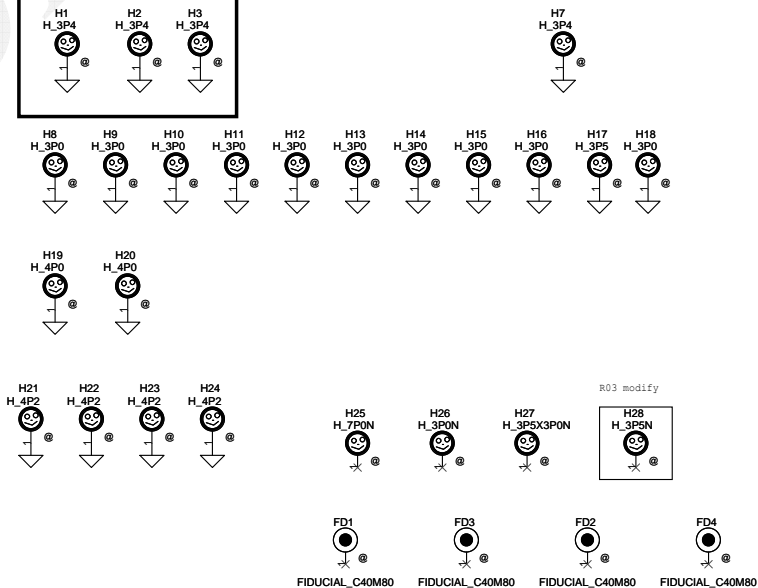
Singatron 2SJ2326
DC021007151



FAN Stand-Off

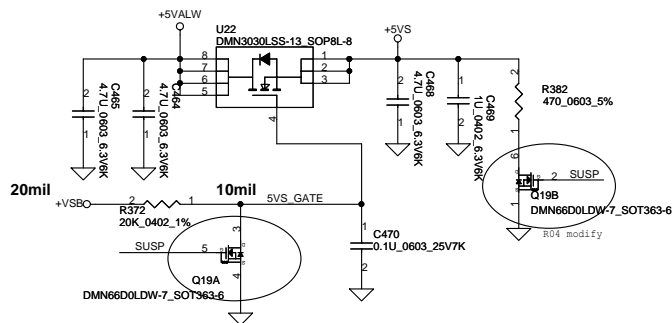


JUSB3 Stand-Off

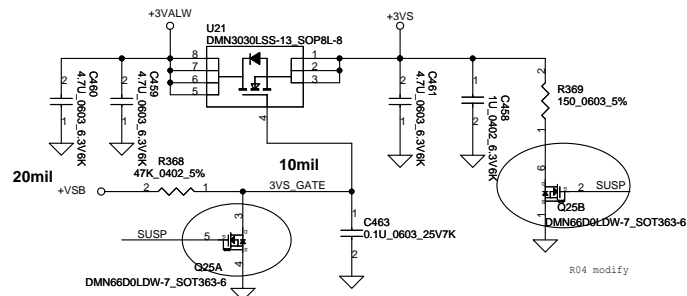


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				Date: Friday, February 10, 2012	Sheet 43 of 63

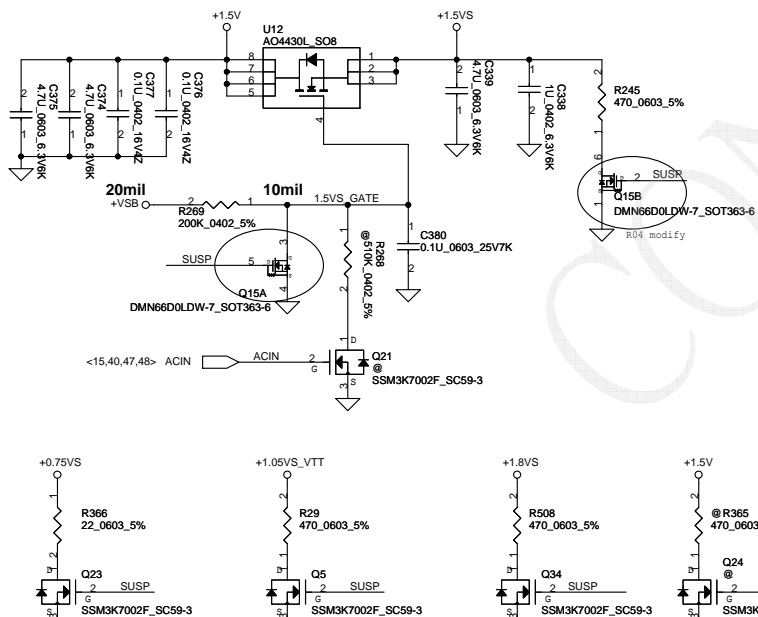
+5VALW TO +5VS



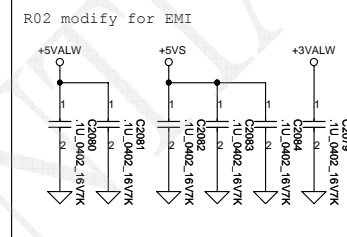
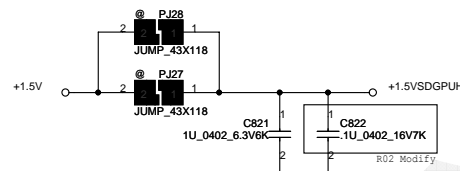
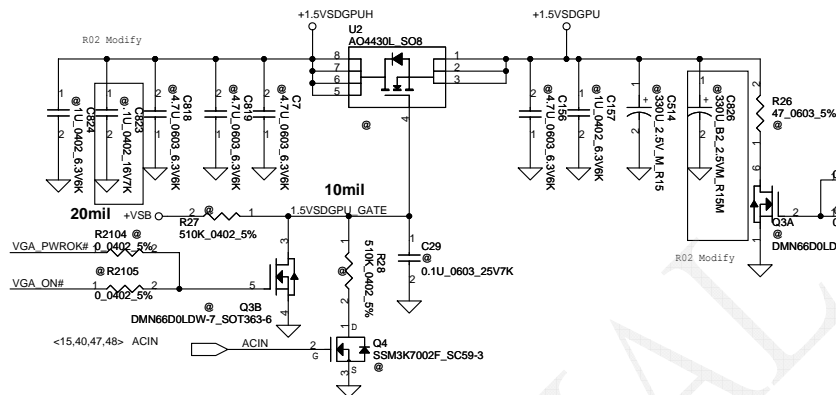
+3VALW TO +3VS



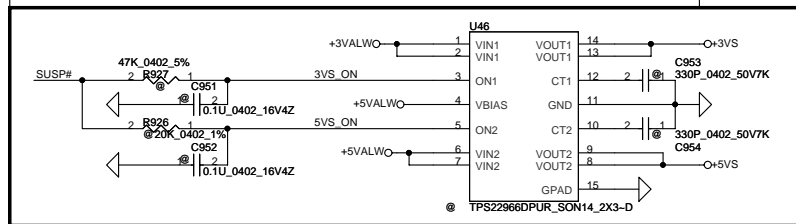
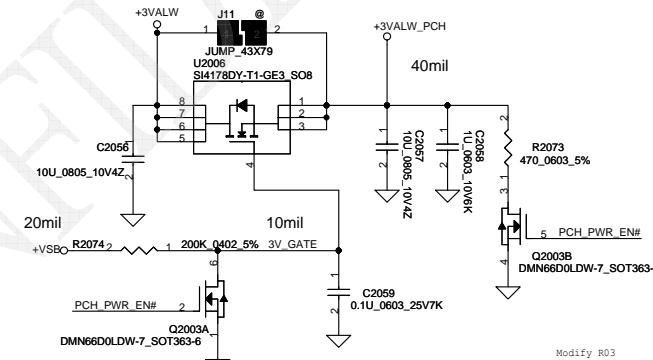
+1.5V to +1.5VS



+1.5VSDGPUH to +1.5VSDGPU for GPU

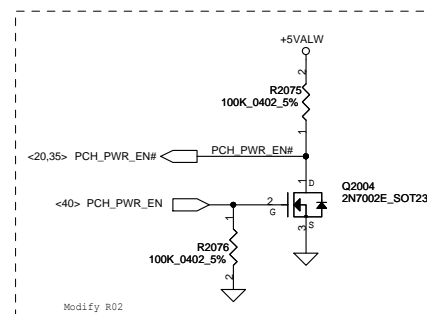
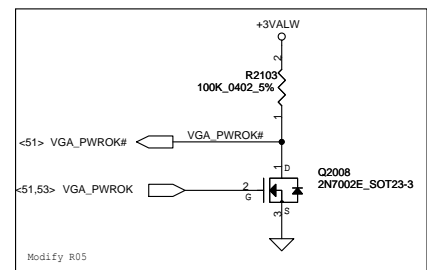
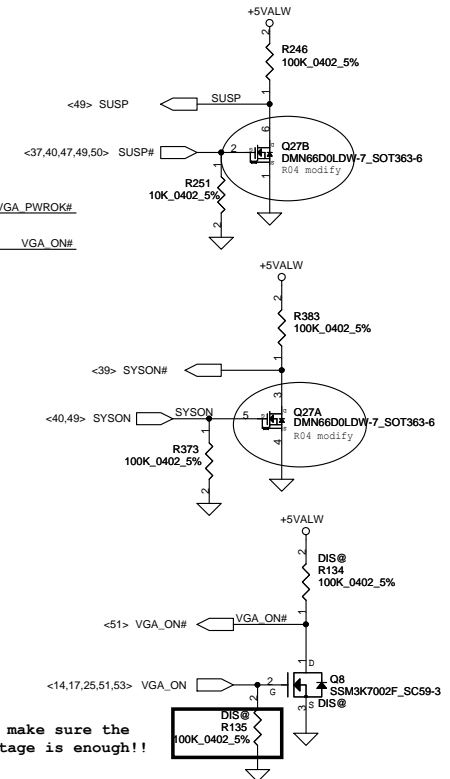


+3VALW TO +3VALW(PCH AUX Power)



Reserved

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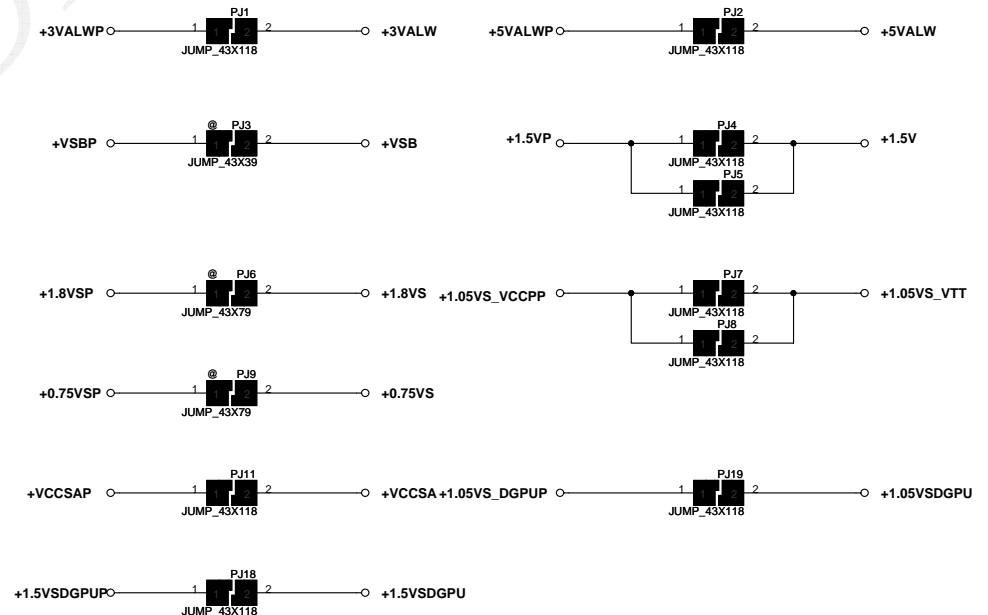
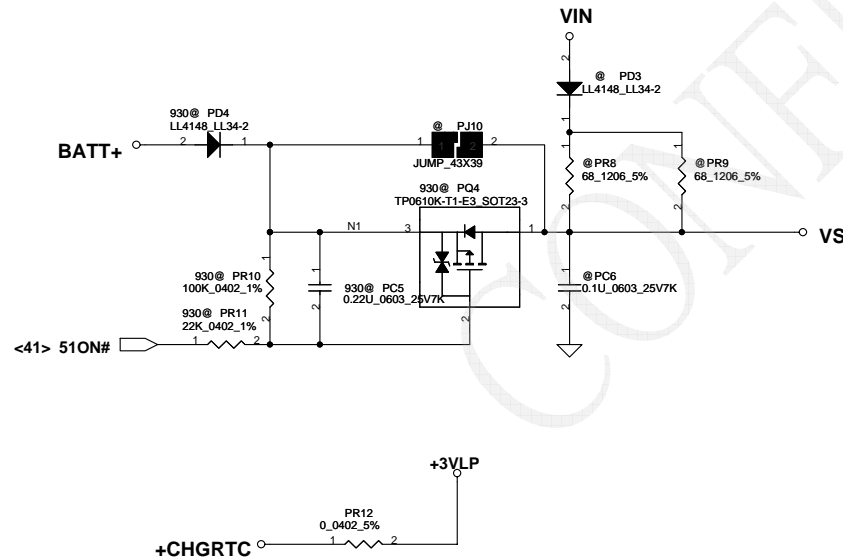
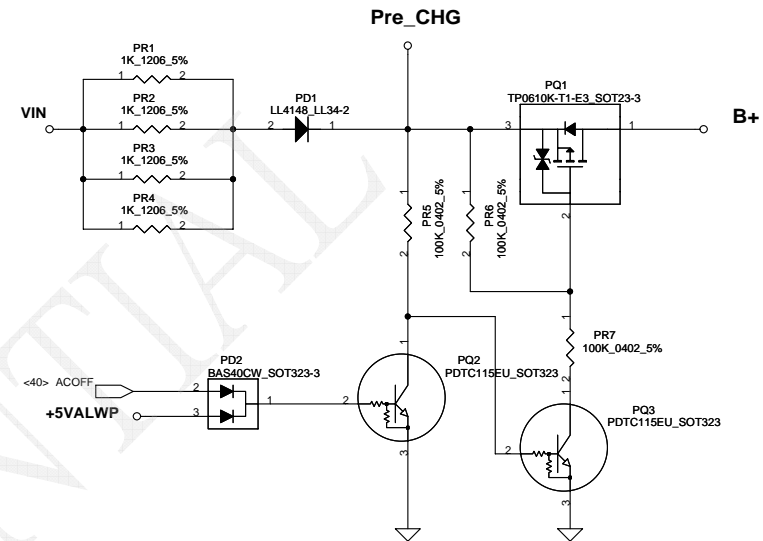
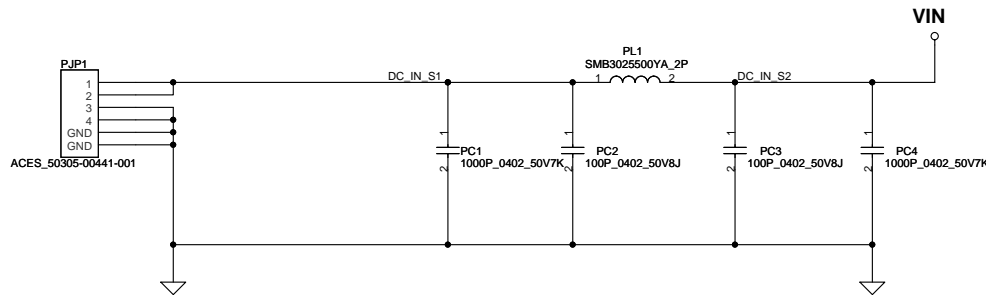


Compal Electronics, Inc.

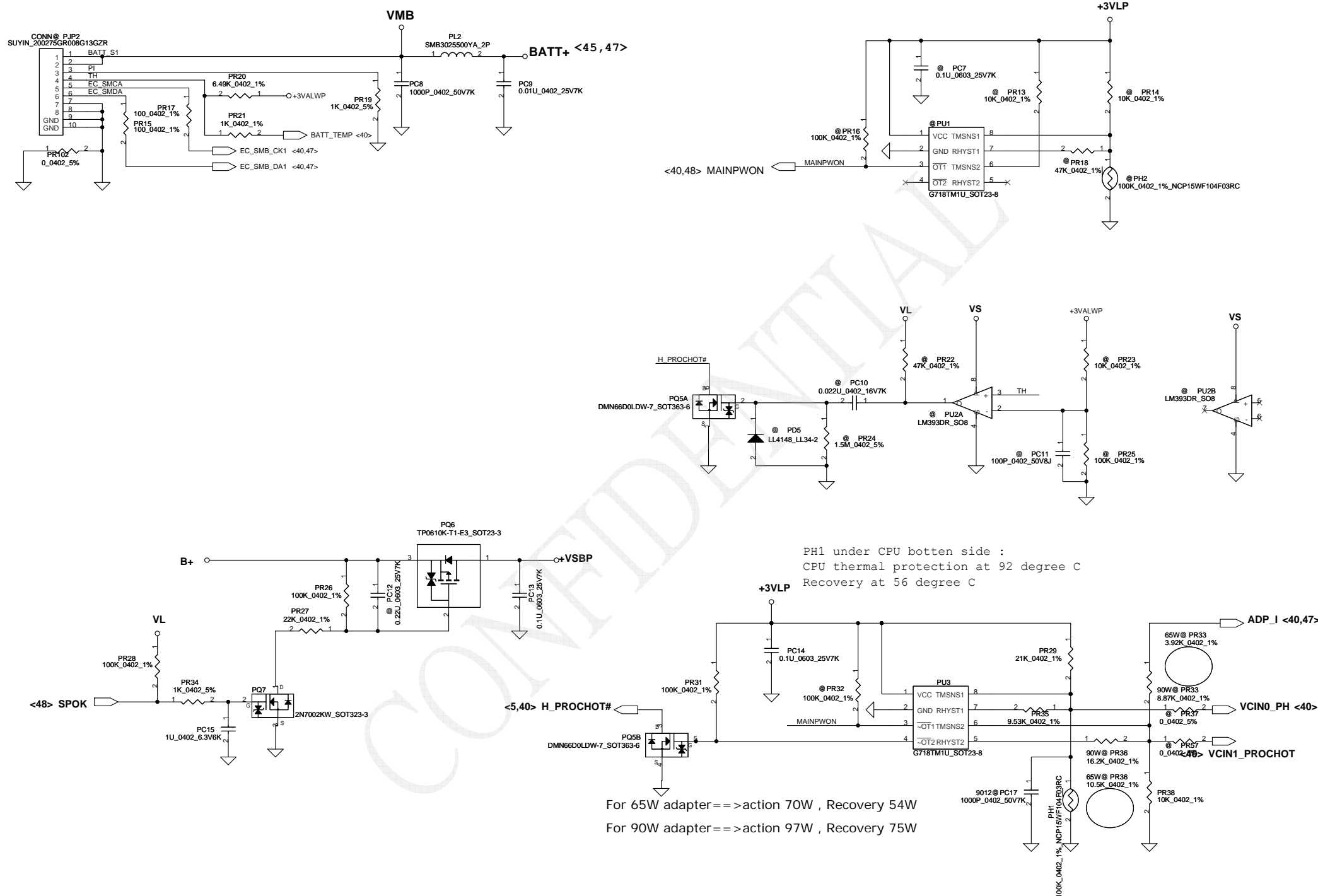
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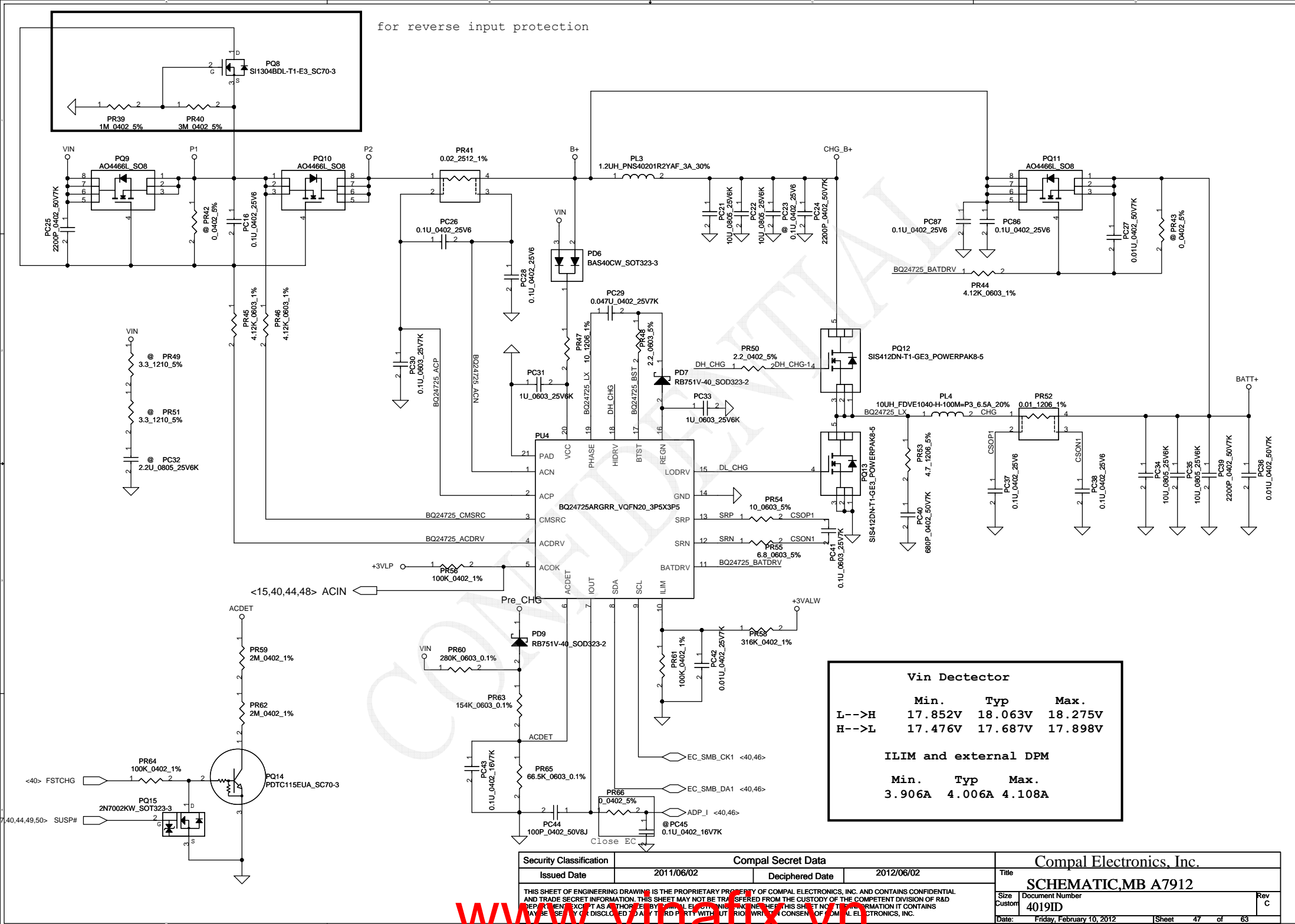


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				Customer					
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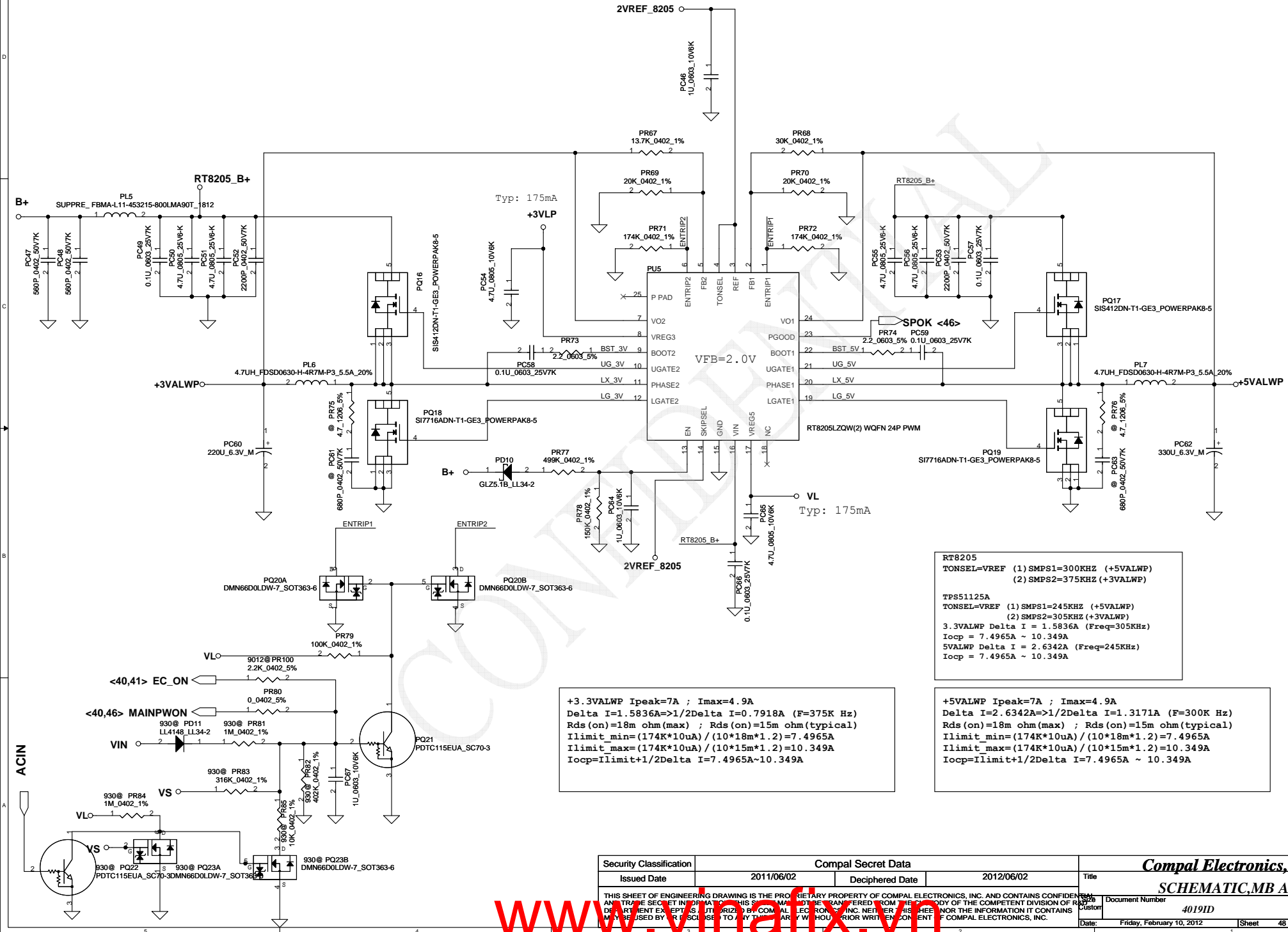


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for reverse input protection

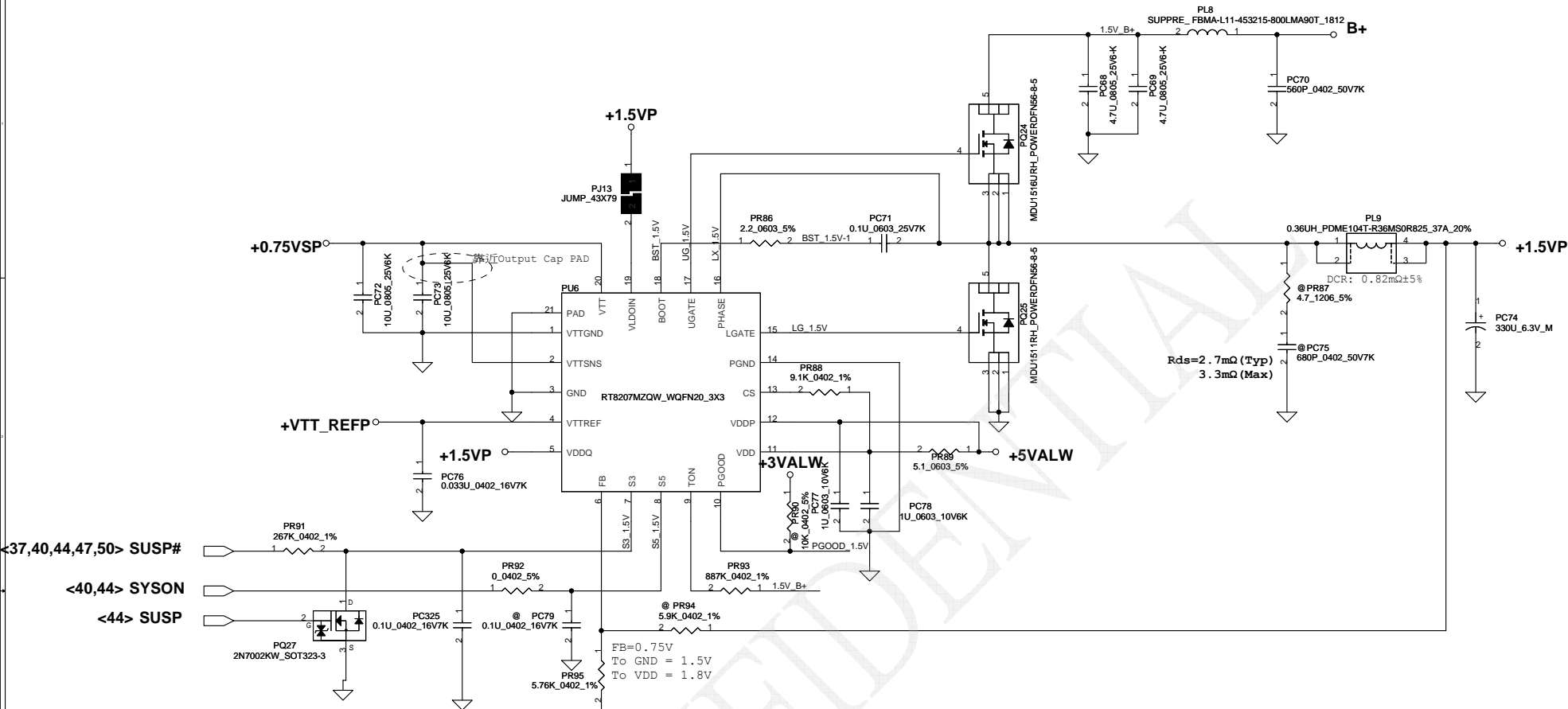


Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



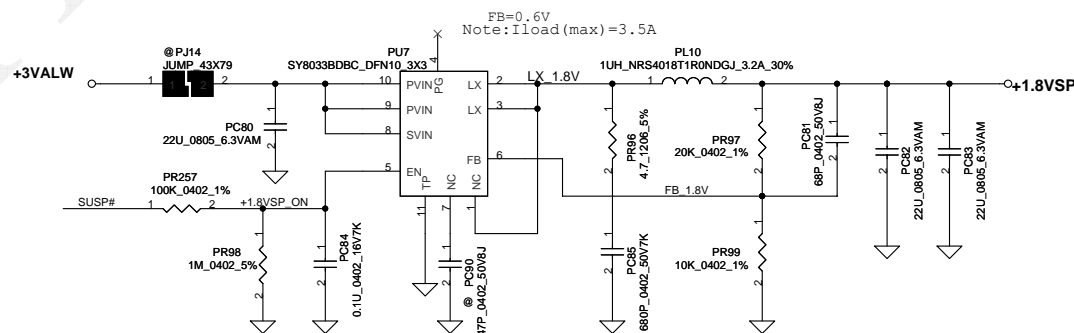
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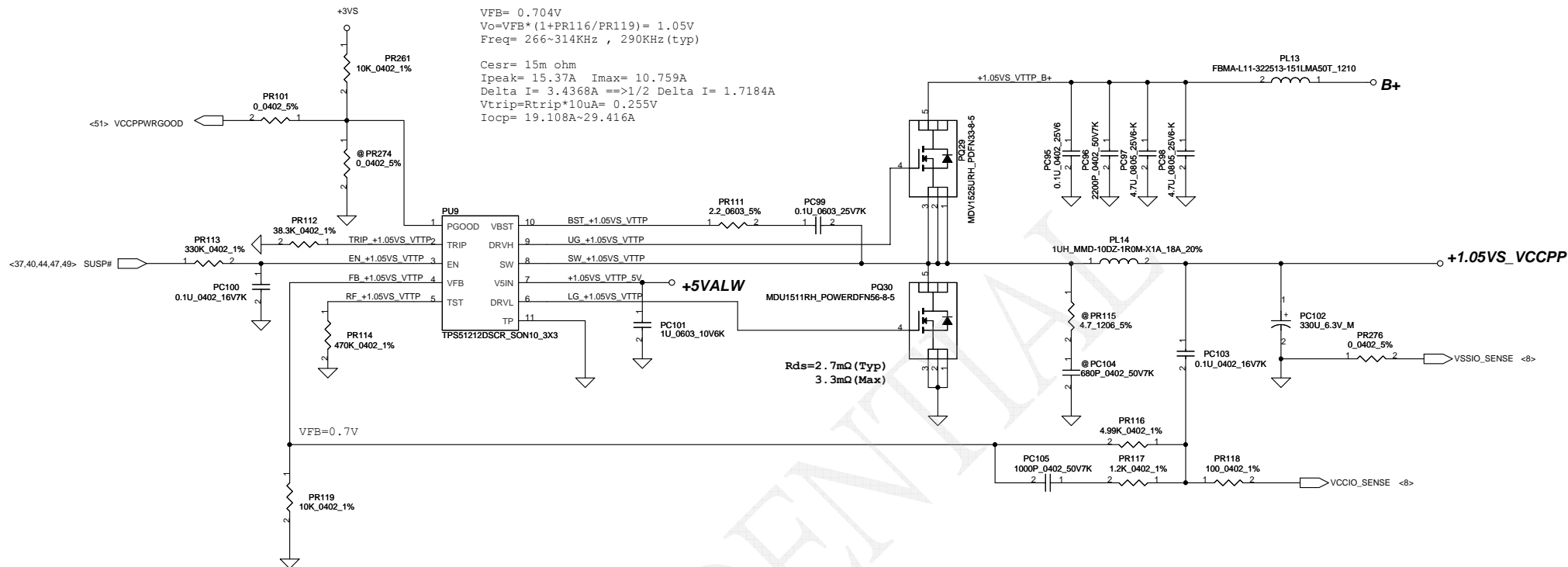


STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

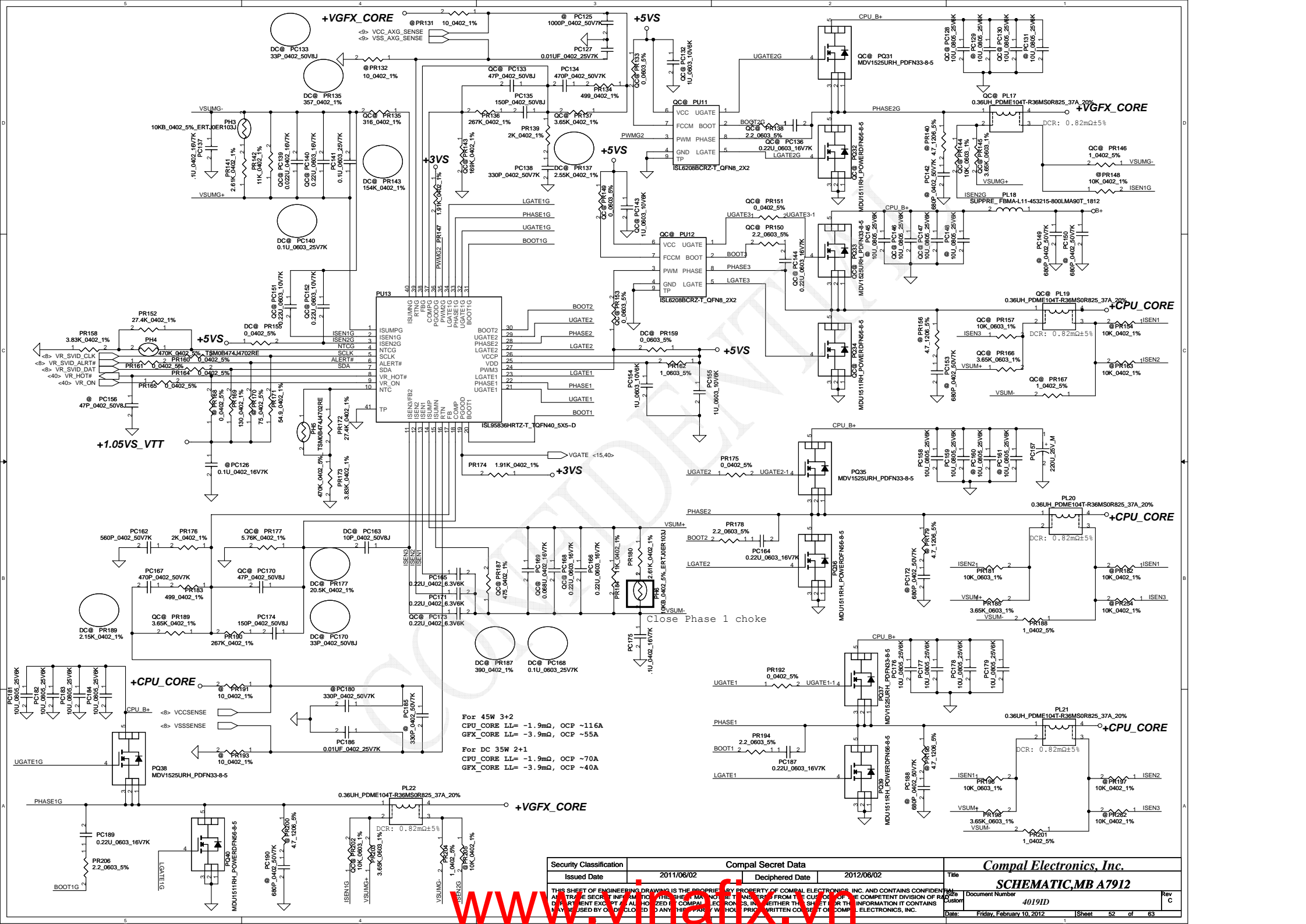
Note: S3 - sleep ; S5 - power off



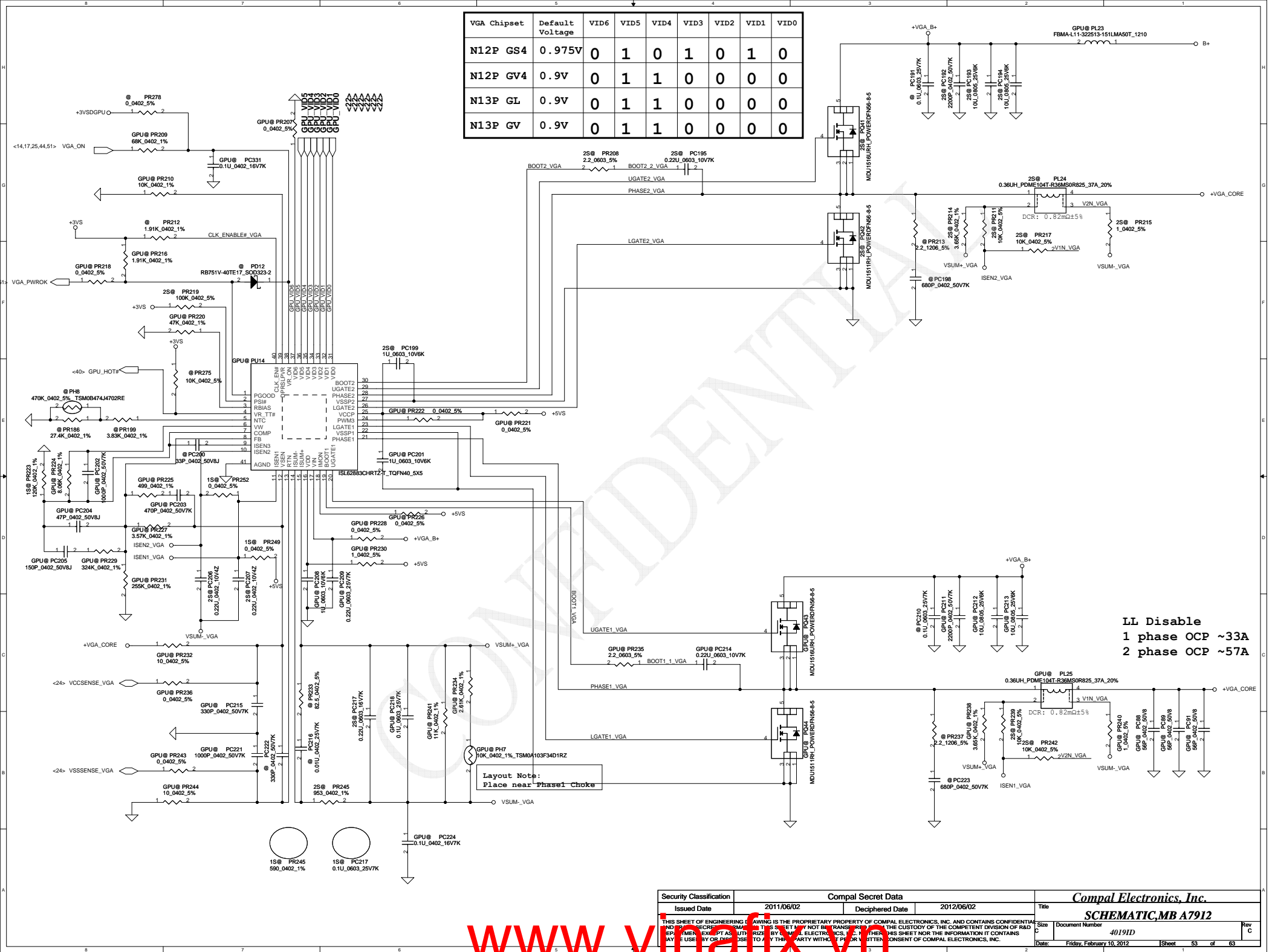
Notice: Internal resistance about 500K on 2nd EN pin



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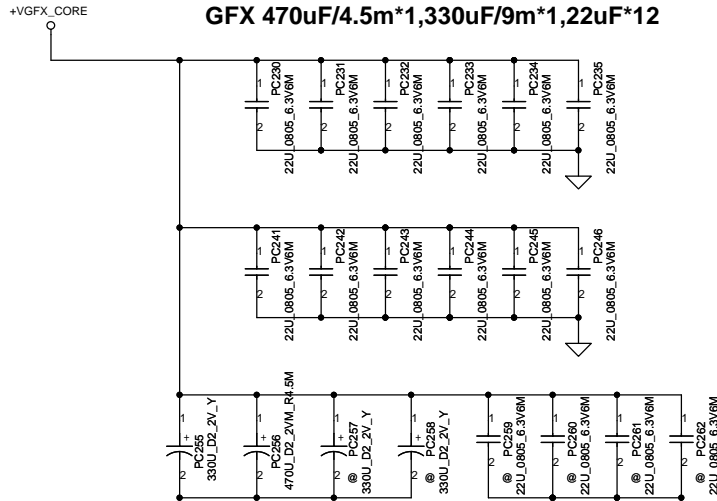


VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0



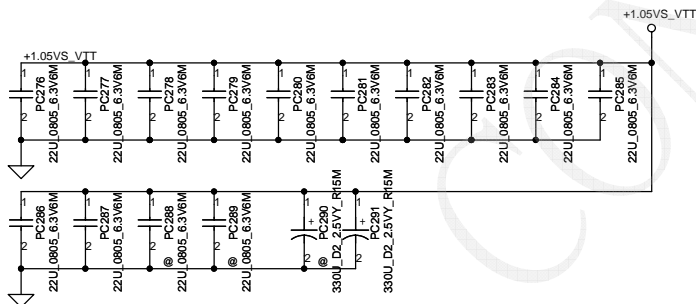
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PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

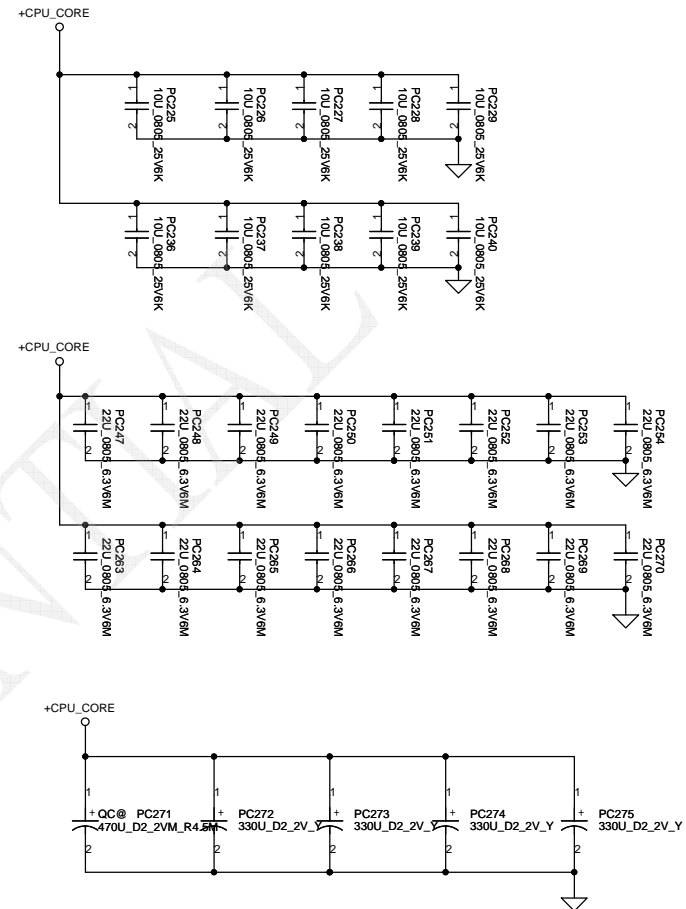


Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

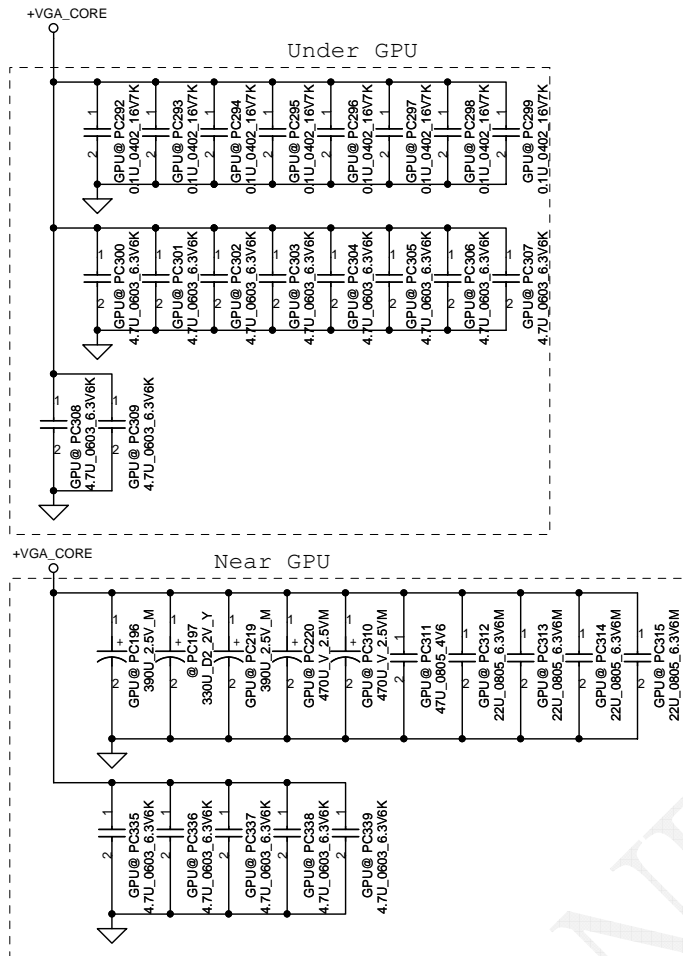


INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0



DC@ PC271
 330uF 0805 6.3V6M

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2	2011 1208	DVT
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	PVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	PVT
8		Consider part rating		51	Change PR277 from 0402 to 0603	2011 1222	PVT
9		Tune transient character		52	Add PC139, PC169 Swap PC271 & PC275	2011 1222	PVT
10		PH1 OTP and ADP_I throttling by H/W control		46	Delete PR37, PR57	2011 1222	PVT
11		Follow Power design		55	Add PC313, PC314, PC315	2011 1222	PVT
12	VGA sequence meet nVidia SPEC			51	Swap PR258 & PR263, PR266 & PR264, PR246 & PR265	2011 1223	PVT
13	Cut-in EMI solution			47	Add PR53, PC40	2012 0104	PVT2
10							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
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1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add f11009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	Add USB chargeaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)		0.2
7	P.44		9/7	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU_ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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25	P. 44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P. 36		9/20	HW	For SD3.0 issue (Add R2088,R2089)		0.2
27	P. 20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P. 44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P. 40		10/17	HW	Board ID error. Add R353.		0.3
30	P. 40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P. 17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P. 18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P. 13.40		10/25	HW	Co lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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43	P. 41		11/16	ME		Delete SW5, SW6, Pop SW2, SW3	0.4
44	P. 05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P. 35		11/17	HW	LAN SPROM on Chip	De-pop U31, R537 Pop R538	0.4
46	P. 36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P. 13		11/17	HW	RTC issue	Change C682, C686 to 15P	0.4
48	P. 31, 32, 41		11/17	ESD		De-pop D3, D4, D17, D18, D15 Pop D24, D36	0.4
49	P. 40		11/17	HW		De-pop R891, R893	0.4
50	P. 24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P. 13		11/21	HW		Chip Select Change R651, R2049 to 0ohm	0.4
52	P. 13, 40		11/21	HW		Delete NPCE885N (R2091, R2092, R2094, R2095, R2096, R698, R699, R692, C2085)	0.4
53	P. 45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P. 35, 36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525, R536, R537, R538 to 1k	0.4
56	P. 13		11/23	HW		Delete R2093, R2049, R651 (0ohm)	0.4
57	P. 13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P. 35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P. 36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4

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58	P.24.25		12/02			Change R1057 from 35kohm to 45kohm Change R1077 from 40.2ohm to 42.2ohm Change R1080 from 60.4ohm to 51.1ohm	0.4
59	P.22		12/02			for N13P_GS, the boot voltage is 0.9V pop R1022,R1021,R1036,R1035,R1034,R1033 for N13P_GL, the boot voltage is 0.95V pop R1022,R1037,R1020,R1019,R1034,R1033 for N13M_GS, the boot voltage is 0.925V pop R1022,R1037,R1020,R1019,R1018,R1033	0.4
60	P.44		12/02			Change R369 from 470ohm to 150ohm Change R26 from 470ohm to 47ohm Pop Q3	0.4
61	P.13		12/02			BIOS ROM(4M) Change U36 to SA00003K800	0.4
62	P.35		12/06			EMI suggestion for Card Reader Change R195 from 33ohm to 22ohm Change R216 from 22ohm to 0ohm Change C2094 from 6pF to 6.8pF Change R2101 from 0ohm to 22ohm Change R2088 from 47ohm to 75ohm Change R2102 from 47ohm to 0ohm De-pop C2096	0.4
63	P.36		12/07			EMI request for 家電下鄉 Add C2097	0.5
64	P.39		12/07			For PCH HM70 Change USB port0 to co-lay USB3.0 Change USB port2 to USB2.0 Change USB port 11 to BT	0.5
65	P.44		12/07			Change 1.5VSDGPU_EN from VGA_ON# to VGA_PWROK# Add R2103,Q2008	0.5
66	P.18		12/09			For eDP Change Q2007 from SB501380020 to SB501110010	0.5

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67	P.31		12/16	EE		change Q2007 to 2N7002 for eDP_HPD circuit	LA-7912 0.2
68	P.40		12/16	EE		add WLAN_PME# on pin85. add wlan_on signal on EC pin38 add AC circuit	LA-7912 0.2
69	P.35		12/16	EE		reserve Q2007 for open +3V_LAN by PCH_PWREN#	LA-7912 0.2
70	P.40		12/16	EE		add R2063 for pull high VCIN0_PH to +3VL 10k add R2059 for pull low VCIN1 10k	LA-7912 0.2
71	P.41		12/20	EE		resever R2116 ~ R2119 for change LED power to 3VLA-7912 resever C2101~C2107 56pF on T/P for EMI	0.2
72	P.36, 14		12/22	EE		change R384 & R385 power to +3V_LAN unpop R630 & reserve R2120 to pull high +3V_LAN	LA-7912 0.2
73	P.42, 35		12/22	EE		change Q43 from 2n7002 to BSS138 unpop R209	LA-7912 0.2
74	P.40		12/23	PWR		change R353 to 56k for board ID 0.2 power request pop R2063, R2059 un-pop R880, R891, R893	LA-7912 0.2
75	P.39		12/23	EMI		change USB3 signal pass by chock (SM070001600)	LA-7912 0.2
76	P.41		12/23	ME		Change LED(Blue) SC591NB5A30 to SC591TBKA10 Change LED(AMBEL) SC500007700 to SC500005930 change (R2116=130ohm), (R377,2118,378=390ohm) (R2117,2119 = 51 ohm)	LA-7912 0.2
78	P.36		12/23	EMI		R2088 change to 10ohm	LA-7912 0.2
79	P.25		12/23	EMI		L1002 use SM010028800 (for N13P_GL) use 0ohm on N13P_GS,N13M_GS	LA-7912 0.2
80	P.44		12/24	EE		POP R2104, R2106 unpop R2105, R2107 for VGA sequence	LA-7912 0.2
81	P.41,24		12/24	EMI,EE		De-pop C217,C216 EMI request. add R1019, R1020, R1037 for GM@ (VGA_CORE)	LA-7912 0.2
82	P.40,27		12/27	EE		change R2059&R2063 to 10k ohm for EC request C2086~C2089 change bom sturte to DIS@	LA-7912 0.2
83	P.40		12/27	EE		add R2125, R2123 for option WL_OFF# to EC or PCH add R2122, R2124 for option BT_ON# to EC or PCH reserve R2126 to pull high 3VALW reserve R2127 to pull high 3VALW	LA-7912 0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
83	P. 41		01/02	EE		reserve R2121 for WLAN_LED connect +3VALW change C2101~2107 bomstucture to GM@	LA-7912 0.3
84	P. 13		01/09	EE		add GPIO23 for define USB config. (R2128 & R2092)	LA-7912 0.3
85	P. 45~56		01/09	PWR		update power circuit	LA-7912 0.3
86	P. 37		01/09	EE		change R2110 to pull high +3VS_FULL	LA-7912 0.3
87	P. 31		01/10	EE		add R2130 reserve for lvds short issue	LA-7912 0.3
88	P. 40		01/10	EE		change board ID to 0.3 (R353 100k)	LA-7912 0.3
89	P. 37		01/11	EE		change R2110 to pull high +3VALW	LA-7912 0.3
90	P. 37		01/11	EE		pop +3VS_FULL 開電線路	LA-7912 0.3
91	P. 13		01/11	EE		add new bom structer usb2@ for usb flag	LA-7912 0.3
92	P. 44		01/11	EE		UNPOP +1.5VSDGPUH to +1.5VSDGPU circuit	LA-7912 0.3
93	P. 35, 40		01/12	EE		add R2131,R2132 for option turn off 3VLAN power by PCH_PWR_EN# or LAN_PWR_EN# (from EC)	LA-7912 0.3
94	P. 37, 40		01/18	EE		add R2134~R2136 reserve for AOIC for ACER request	LA-7912 0.3
95	P. 17		01/18	EE		reserve R2137 pull low USB_P8 for PCH leakage	LA-7912 0.3
96	P. 32		02/02	EE		change R428 & R426 to 0 ohm for CRT issue	LA-7912 0.3

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