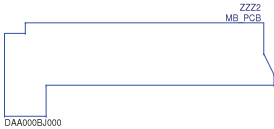


MODEL NAME : Celtic  
PCB NO : LA-D312P  
BOM P/N :



	R1	R3	R3	R3	R3
CPN	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000	DAA000BJ000

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Schematic Document

Celtic (Skylake Y)

2015-12-10

Rev: 1.0

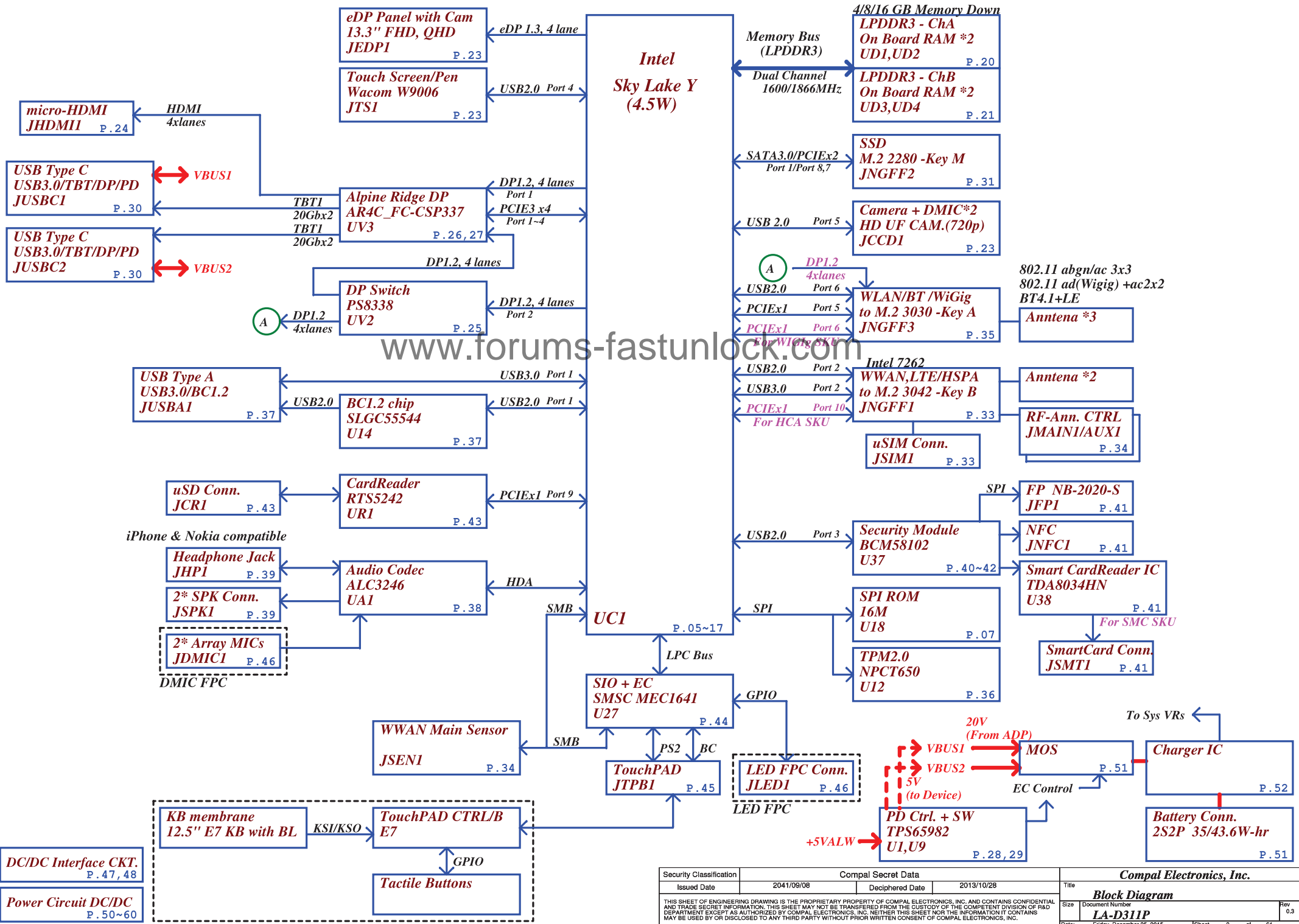
AR Option

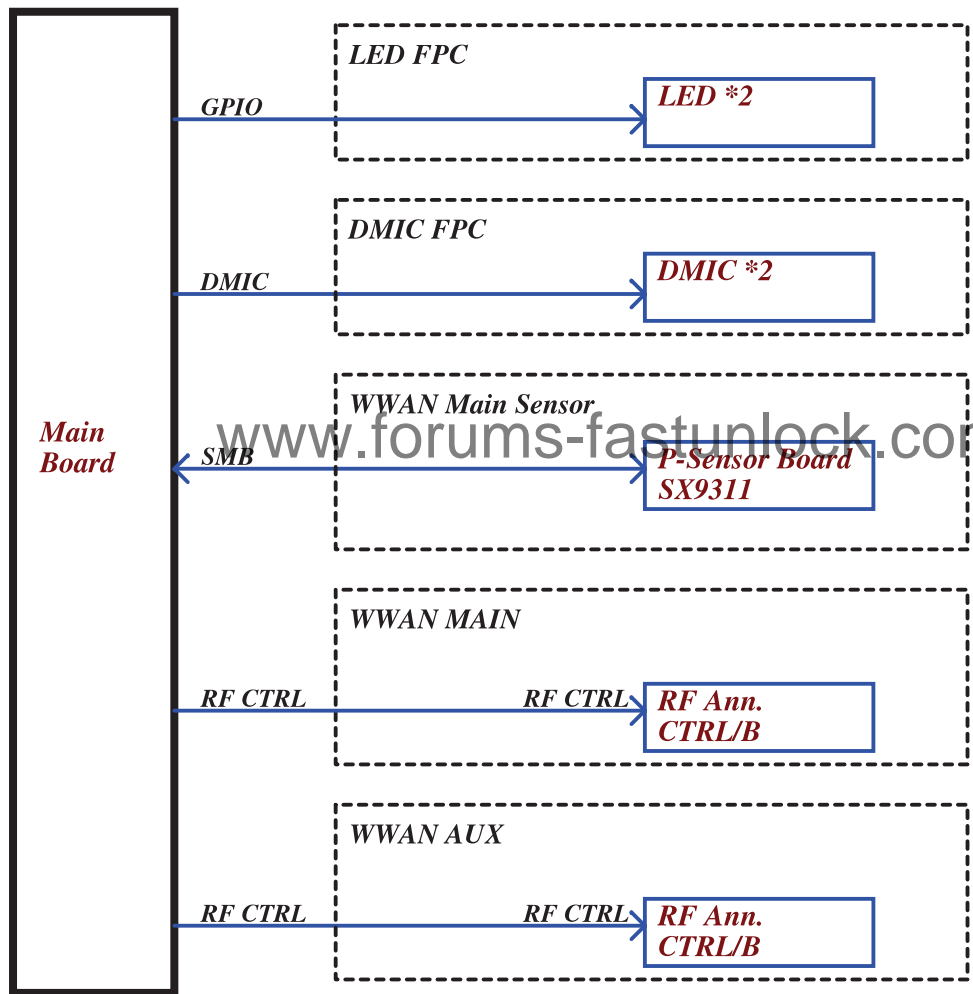


CPU Option



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		LA-D311P			0.3
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ Power plane	+3VALW_DSW +3VALW +1.8VALW +3VLP	+3VPRIM +1.8VPRIM +1.0VPRIM +1.0VAGATE +0.95VPRIM	+1.2VDDR +3.3VCV2 +1.8VMEM +1.0V_VCCST	+5VS +3VS +1.8VS +1.0V_VCCSTG +0.85VS_VCCIO +0.6VS_VTT +VCC_SA +VCC_GT +VCC_CORE
S0	ON	ON	ON	ON
S3 / AC	ON	ON	ON	OFF
DS3	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	BATT	Charger	XDP	USH	PD Controller -1	PD Controller -2	GPIO Expander	P-sensor
PCH_SML0CLK PCH_SML0DATA	PCH								
PCH_SML1CLK PCH_SML1DATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH			V					
EC_SMB00_CLK EC_SMB00_DAT	MEC1641								
EC_SMB01_CLK EC_SMB01_DAT	MEC1641				V				V
EC_SMB03_CLK EC_SMB03_DAT	MEC1641	V							
EC_SMB04_CLK EC_SMB04_DAT	MEC1641		V						
EC_SMB05_CLK EC_SMB05_DAT	MEC1641					V			
EC_SMB07_CLK EC_SMB07_DAT	MEC1641						V		

Board ID Table

Vcc	3.3V +/- 5%			
Board ID	R	C	PCB Revision	REV
0	240K +/- 5%	4700p	0.1	EVT1.0
1	130K +/- 5%	4700p	0.2	DVT1.0/DVT1.1
2	62K +/- 5%	4700p	0.3	DVT2.0/PreMP
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		
6	2K +/- 5%	4700p		
7	NC			

SOC DDI Port Mapping	DDI PORT#	DESTINATION
	B	Alpine Ridge
	C	DP MUX

SOC PCIE Port Mapping	PCI EXPRESS	DESTINATION
	Lane 1	
	Lane 2	
	Lane 3	Alpine Ridge
	Lane 4	
	Lane 5	NGFF (WLAN)
	Lane 6	NGFF (WiGig)
	Lane 7	NGFF (SSD)
	Lane 8/ SATA 1	
	Lane 9	Cardreader
	Lane 10	HCA

Lane reversal

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE1	TBT
	CLKOUT_PCIE2	NGFF (WiGig) or (HCA)
	CLKOUT_PCIE3	Cardreader
	CLKOUT_PCIE4	NGFF (SSD)
	CLKOUT_PCIE5	NGFF (WLAN)

USB 3.0 PORT#	DESTINATION
1	Type A(Debug)
2	WWAN
3	
4	

USB 2.0 PORT#	DESTINATION
1	Type A(Debug)
5	WWAN
7	USH
3	Touch
9	CAM
2	BT

FLEX CLOCKS	DESTINATION
CLKOUT_LPC_0	EC LPC
CLKOUT_LPC_1	Debug

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	sm	0.50000
1	Top		Copper foil	0.33oz+plating	1.20000
			Prepreg	1086	2.65000
2	IN1(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
3	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	1080	2.56000
4	IN2		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
5	GND/PWR		Copper foil	0.5oz	0.60000
			Prepreg	106	1.63000
6	GND/PWR		Copper foil	0.5oz	0.60000
			Core	3mil	3.00000
7	IN3		Copper foil	0.5oz	0.60000
			Prepreg	1080	2.56000
8	GND/PWR		Copper foil	0.33oz+plating	1.10000
			Prepreg	106	1.80000
9	IN4(GND)		Copper foil	0.33oz+plating	1.10000
			Prepreg	1086	2.65000
10	Bottom		Copper foil	0.33oz+plating	1.20000
			SolderMask	sm	0.50000
Overall Thickness (0.8mm ± 10%)					31.85000
					0.80899

Link

Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

⏏ : means Analog Ground

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						Size		Document Number		Rev	
								LA-D311P		0.3	
						Date:		Friday, December 25, 2015		Sheet 4 of 61	

## Functional Strap Definitions

### GPP\_E19 (Internal Pull Down): DDPB\_CTRLDATA

0 = Port B is not detected.

1 = Port B is detected.

### GPP\_E21 (Internal Pull Down): DDPC\_CTRLDATA

0 = Port C is not detected.

1 = Port C is detected.

### GPP\_E23 (Internal Pull Down): DDPD\_CTRLDATA

0 = Port D is not detected.

1 = Port D is detected.

### PU/PD for CPU JTAG signals

+3VALV\_DSW RC9 1 XDR 2 1K 0402 5% XDP HOOK3

+3V PRIM RC2781 XDR 2 100K 0201 5% XDP PRESENT#

+1.0V\_XDP RC2781 XDR 2 1K 0402 5% XDP RST#

+1.0VS\_VCCSTG RC19 2 1 51 0402 5% XDP\_PREQ#

RC20 2 1 51 0402 5% CPU\_XDP\_TMS

RC25 2 1 51 0402 5% CPU\_XDP\_TDI

RC18 2 1 51 0402 5% CPU\_XDP\_TDO

RC40 1 2 2 1K 0402 5% XDP\_ITP\_PMODE

RC23 2 1 51 0402 5% CPU\_XDP\_TCK

RC24 2 1 51 0402 5% CPU\_XDP\_TRST#

CC161 1 2 XDP 0.1U\_0201\_10V6K

CC162 1 2 XDP\_PWRBTN#

RC37 2 1 51 0402 5% PCH\_JTAG\_TMS

RC34 2 1 51 0402 5% PCH\_JTAG\_TDI

RC38 2 1 51 0402 5% PCH\_JTAG\_TDO

RC41 2 1 51 0402 5% PCH\_JTAGX

RC35 2 1 51 0402 5% PCH\_JTAG\_TCK

### <XDP Misc.>

<9,19,44> SIO\_PWRBTN#

<9,19> PM\_SYS\_RESET#

<17> XDP\_ITP\_PMODE

<9,44> PCH\_RSMRST#

### <To CPU JTAG>

### <To PCH JTAG>

CPU\_XDP\_TDO

CPU\_XDP\_TCK

CPU\_XDP\_TDI

CPU\_XDP\_TMS

CPU\_XDP\_TRST#

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CPU\_XDP\_TCK

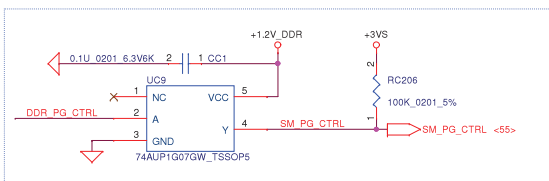
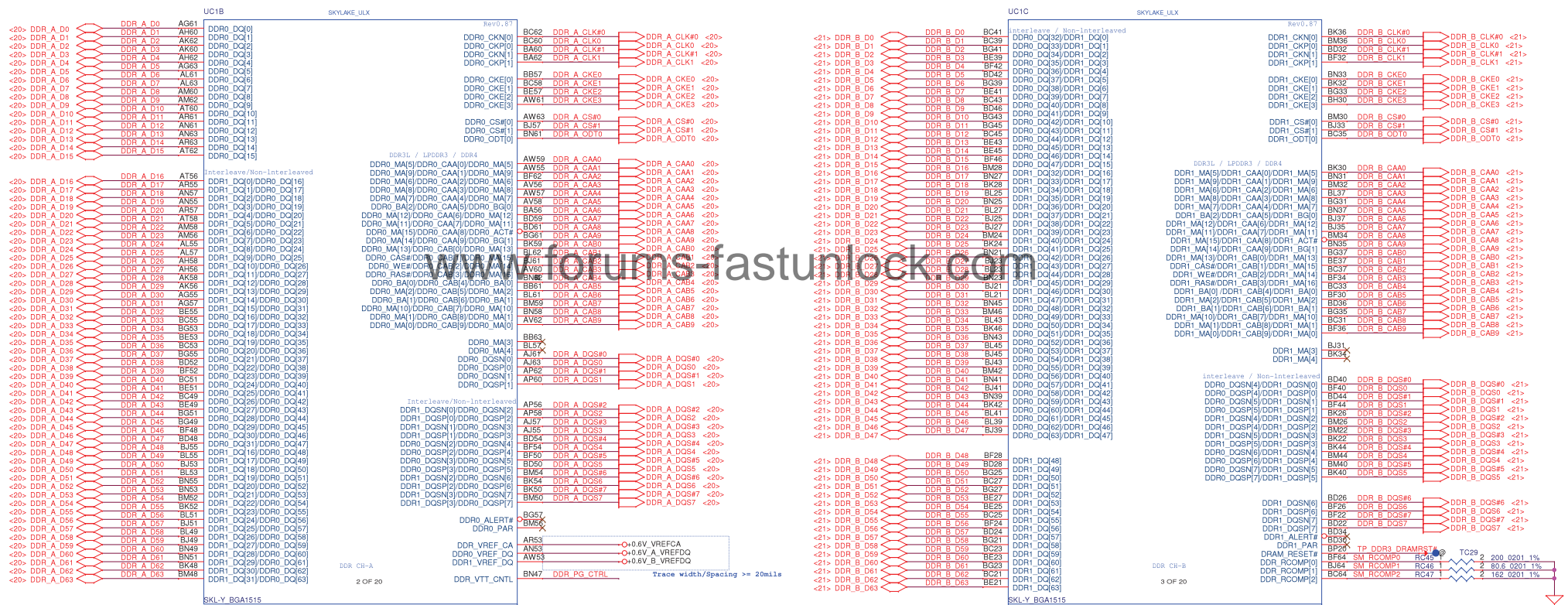
CPU\_XDP\_TDI

CPU\_XDP\_TMS

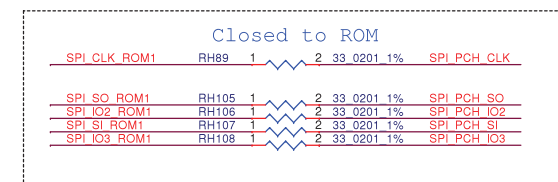
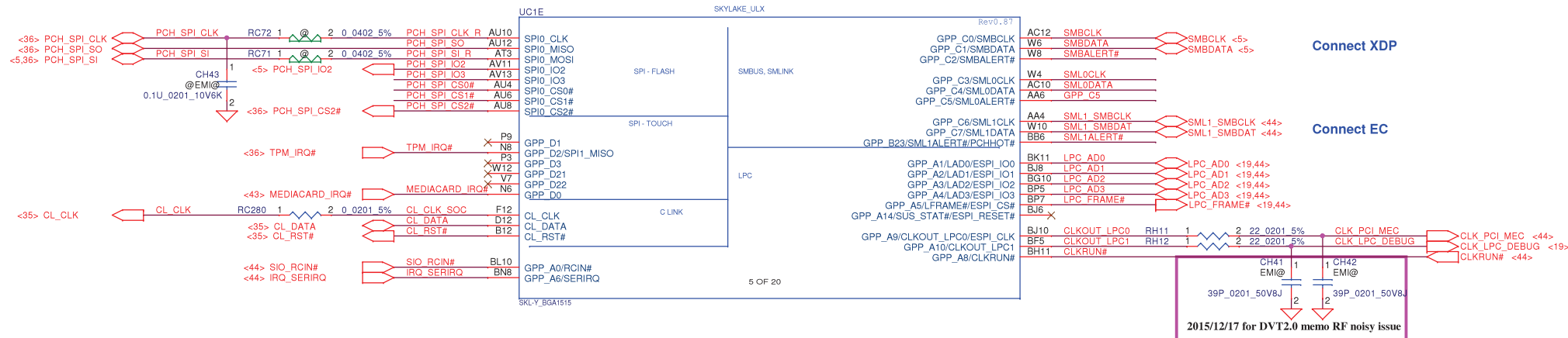
CPU\_XDP\_TRST#



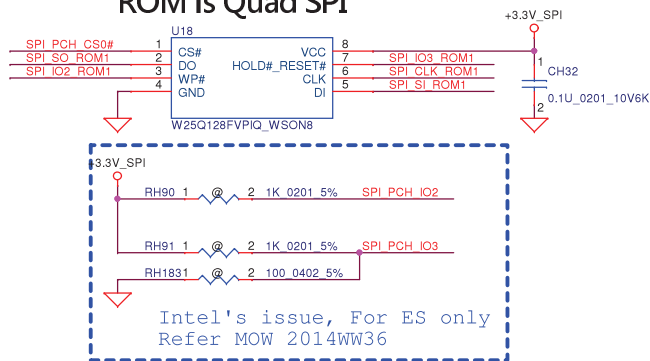
## Non-Interleave Memory



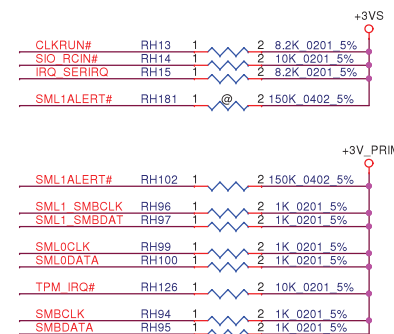
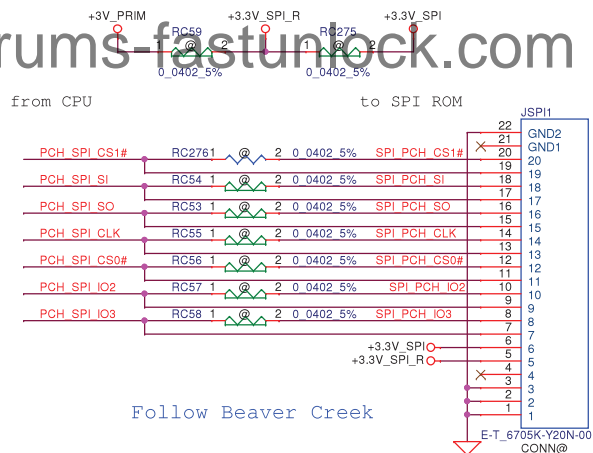
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Issued Date		2041/09/08	Deciphered Date		2013/10/28	Title		
SKL Y(2/13) DDRIII								
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						Size	Document Number	Rev
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## SPI ROM FOR ME (16MByte) ROM is Quad SPI



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## Functional Strap Definitions

GPP\_C2 (Internal Pull Down): SMBALERT#

0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).

1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

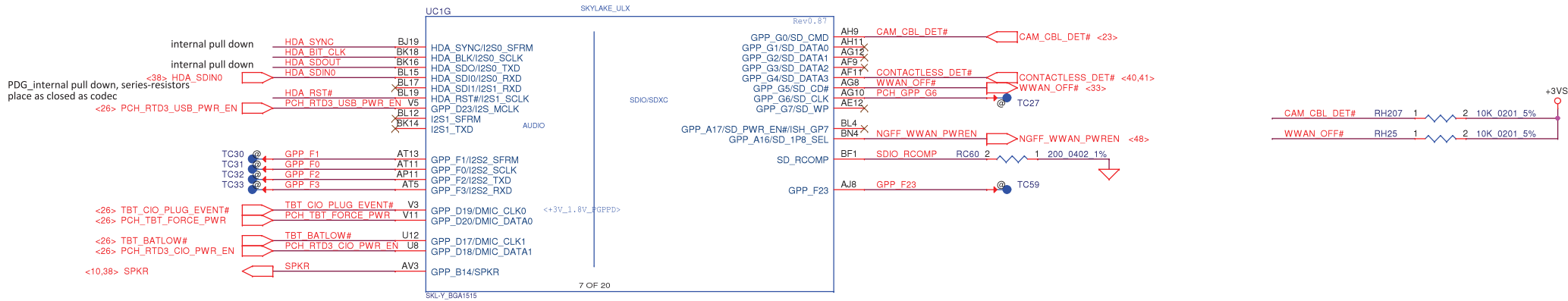
GPP\_C5 (Internal Pull Down): SML0ALERT#

0 = LPC is selected for EC.

1 = eSPI is selected for EC.

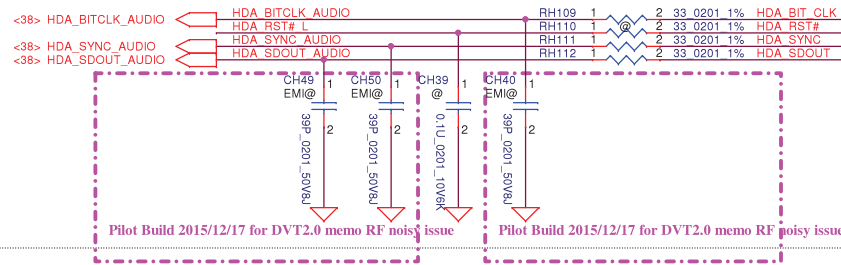
Reserve SO8 footprint for BIOS debug conn  
(SA00005VV00\_W25Q128FVSIG\_SO8)

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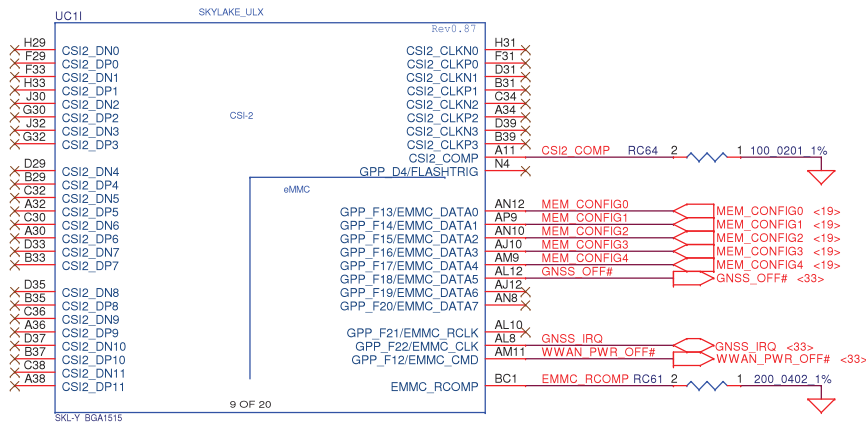
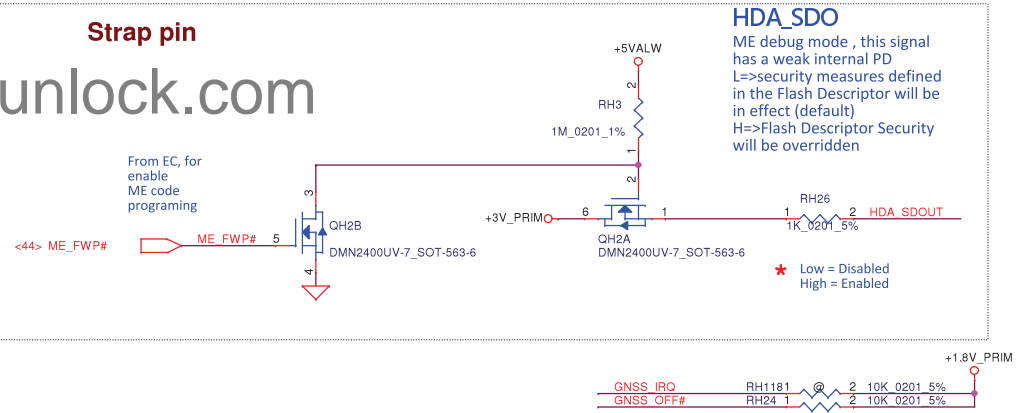


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#### HDA for AUDIO



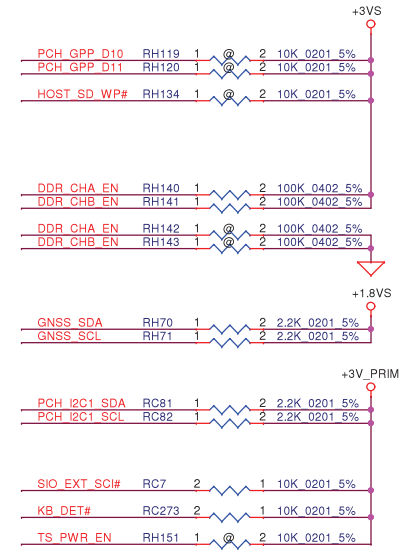
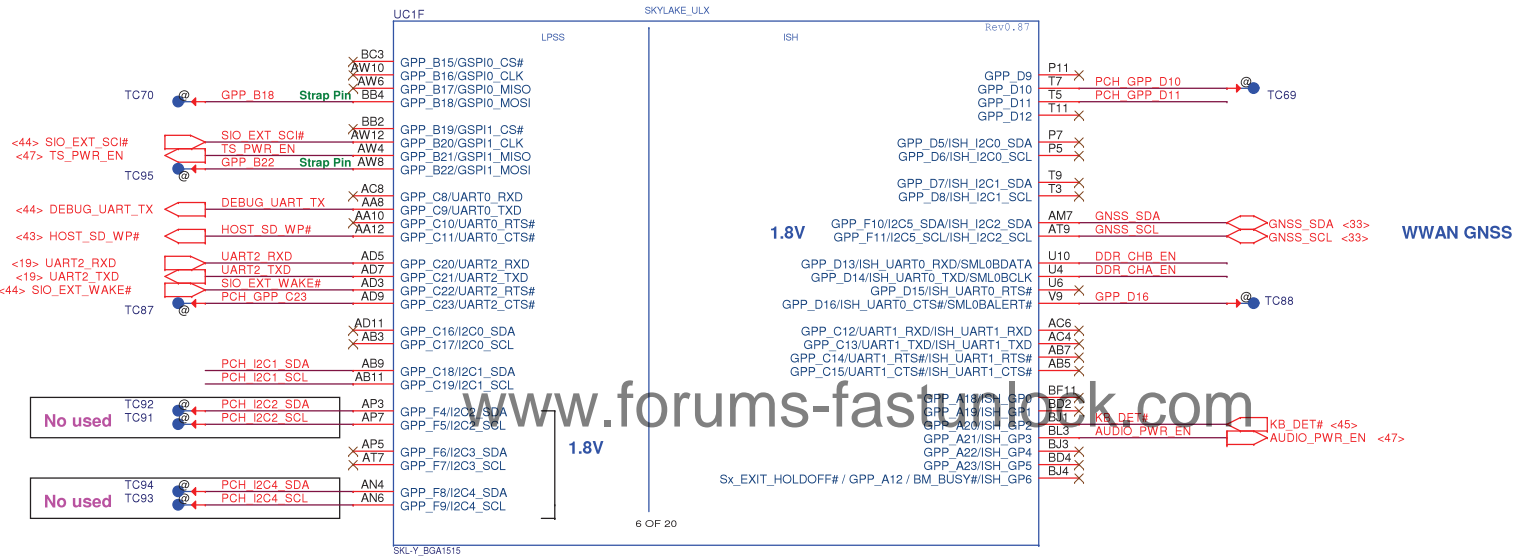
#### Strap pin



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Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	SKL Y(4/13) HDA,EMMC,SDIO
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				Date:	Friday, December 25, 2015
				Sheet	8 of 51







## Functional Strap Definitions

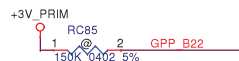
**GPP\_B14 (Internal Pull Down): SPKR**  
**TOP Swap Override**  
0 = Disable TOP Swap mode.----> AAU30 Use  
1 = Enable TOP Swap Mode.



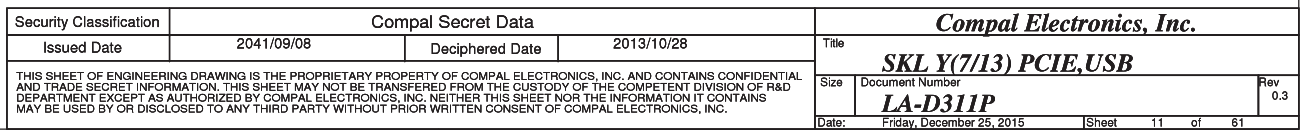
**GPP\_B18 (Internal Pull Down): GSSPI0\_MOSI**  
**No Reboot**  
0 = Disable No Reboot mode. --> AAU30 Use  
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**GPP\_B22 (Internal Pull Down): GSSPI1\_MOSI**  
**Boot BIOS Strap Bit**  
0 = SPI Mode --> AAU30 Use  
1 = LPC Mode



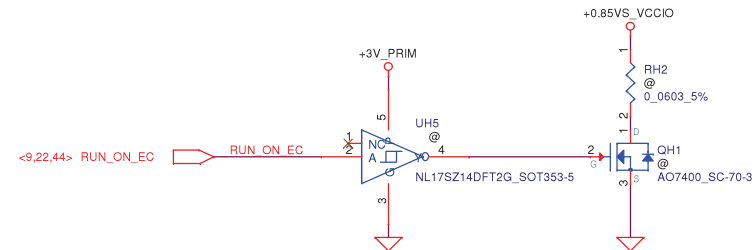
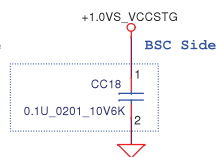
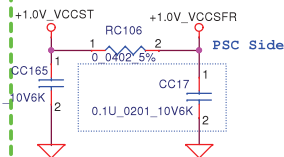
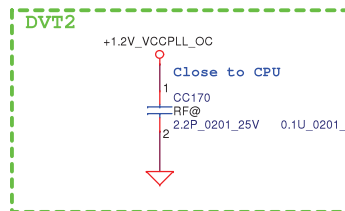
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Issued Date		2041/09/08		Deciphered Date		2013/10/28		Title			
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						Size		Document Number		Rev	
						LA-D311P		0.3			
Date: Friday, December 25, 2015				Sheet		10		of 61			



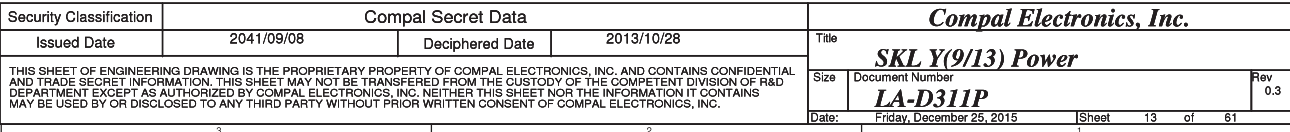
VDDQC trace  
filter width = 6mm  
Total etch length  
= 186.94mils  
PDG P597

VCCST : Sustain voltage for processor standby modes

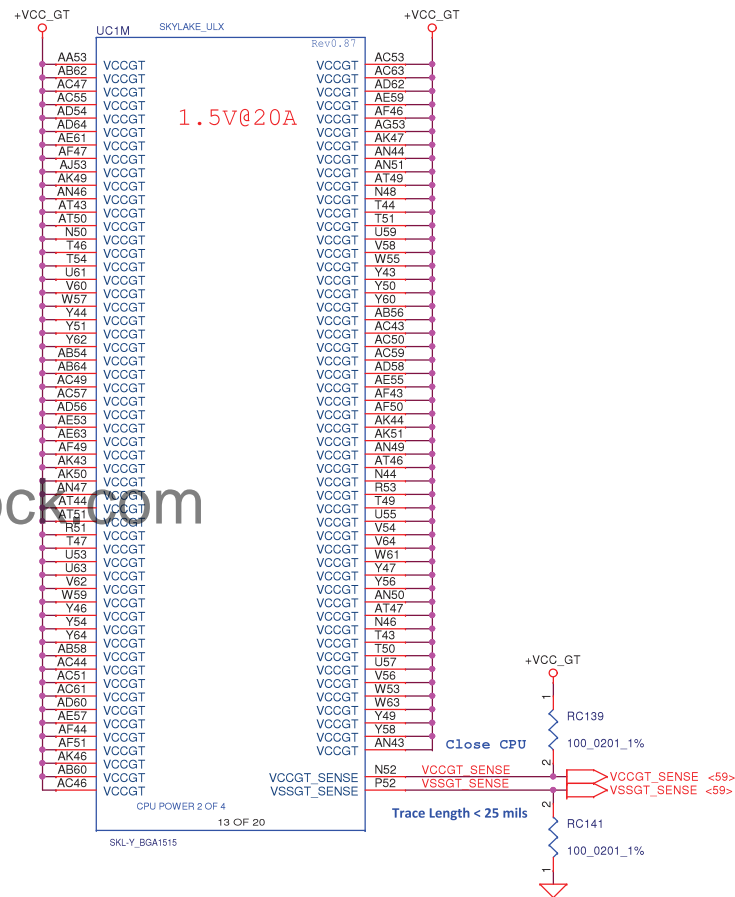
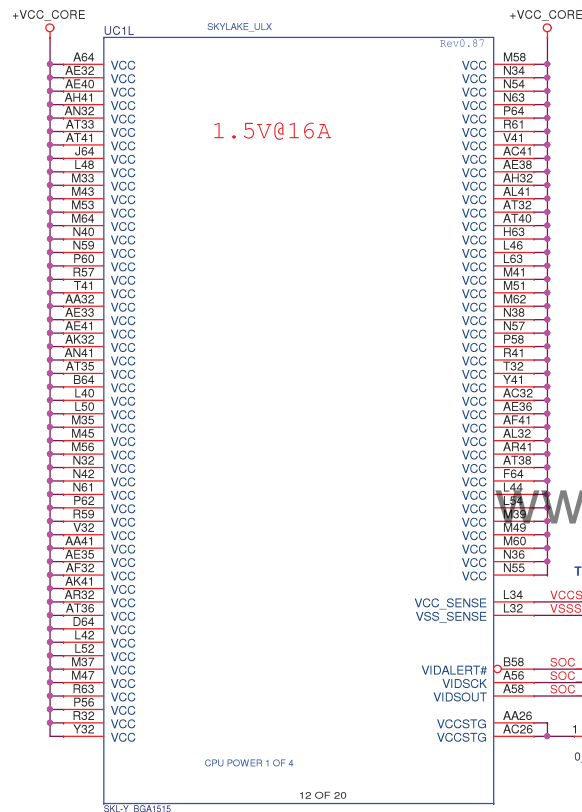
VCCSTG : Gated sustain voltage for processor standby modes



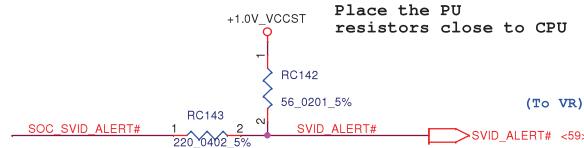
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Size	Document Number	LA-D311P		Rev	0.3
Date:	Friday, December 25, 2015	Sheet	12	of	51



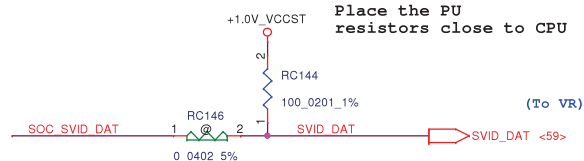




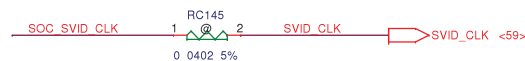
## SVID ALERT



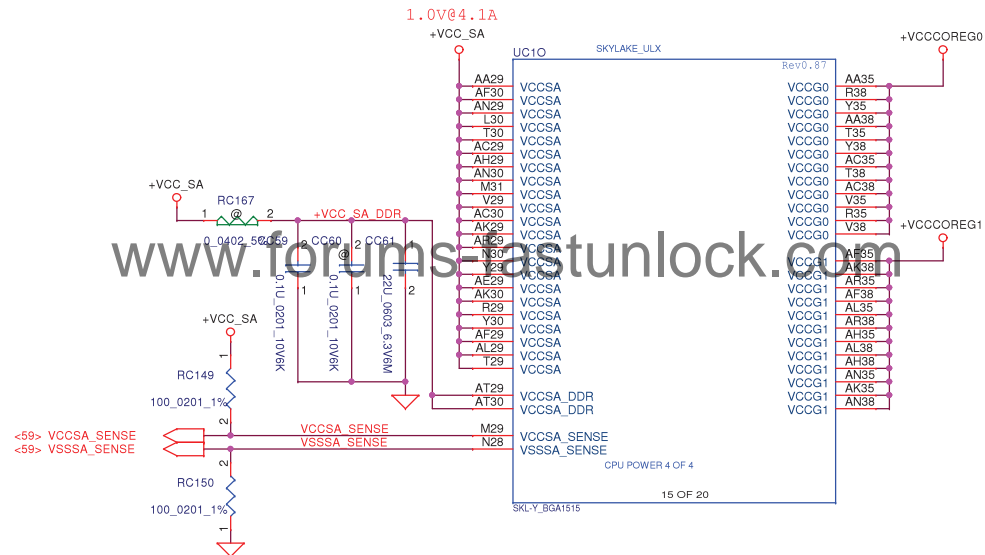
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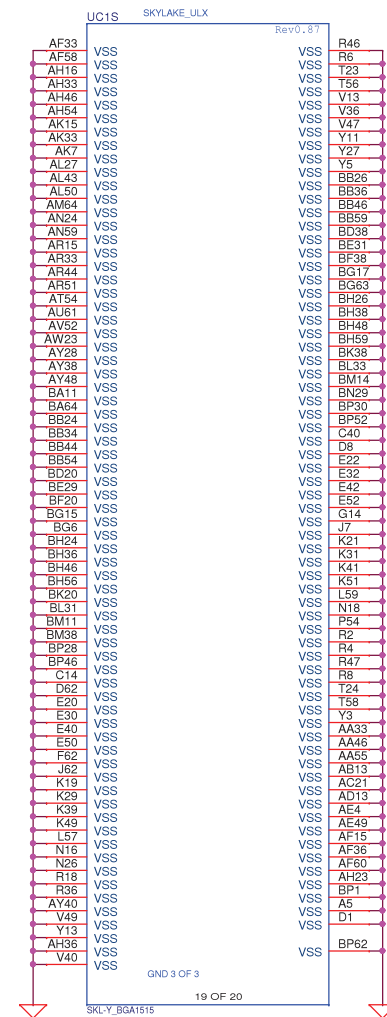
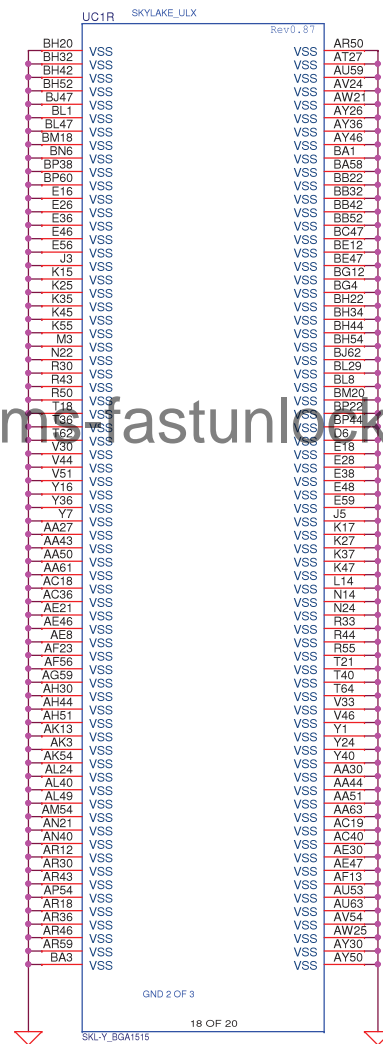
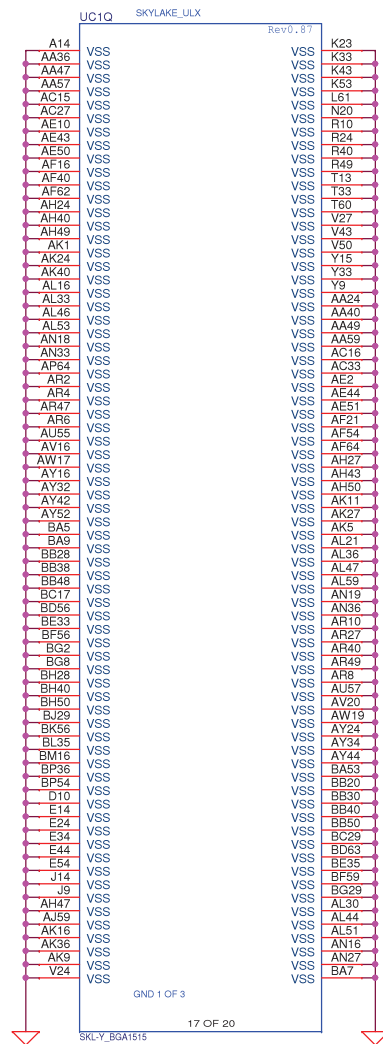
## SVID CLK



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				Sheet	14 of 51
				Rev	0.3

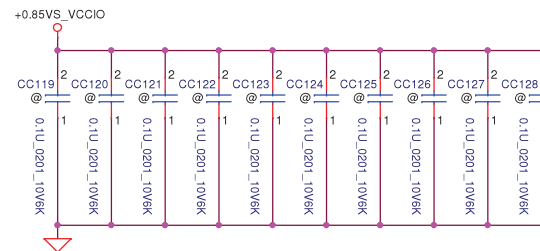
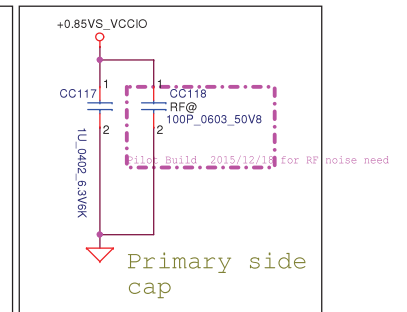
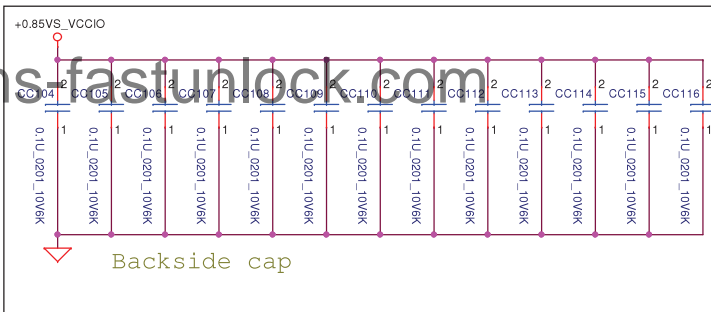
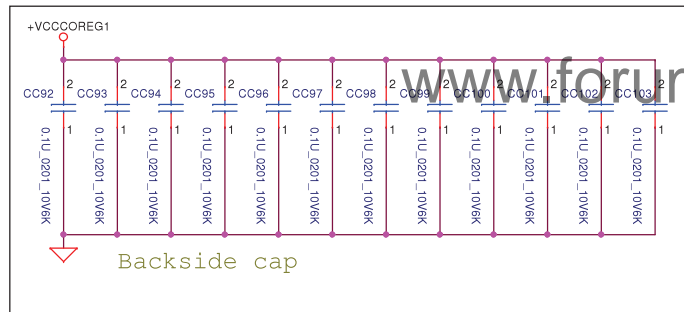
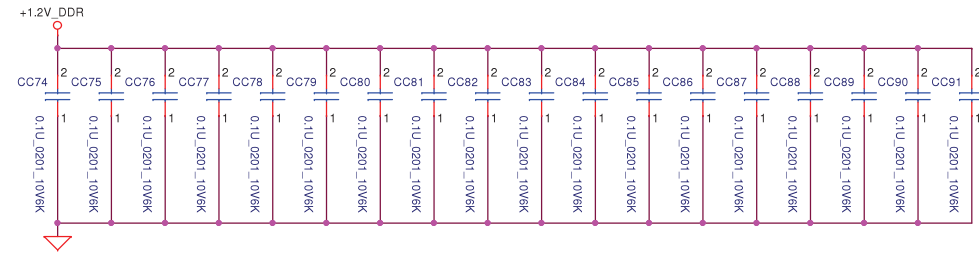
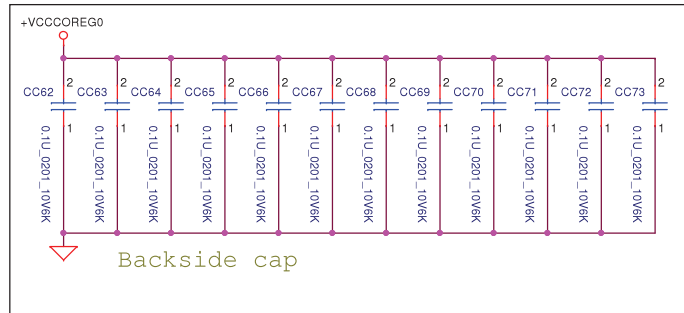


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				<b>LA-D31IP</b>		
				Date: Friday, December 25, 2015	Sheet 16 of 61	0.3

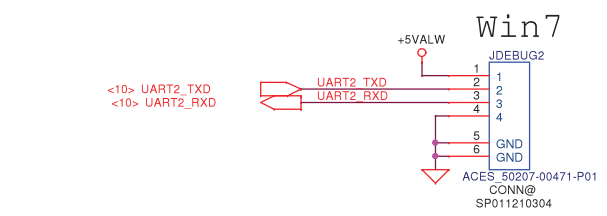




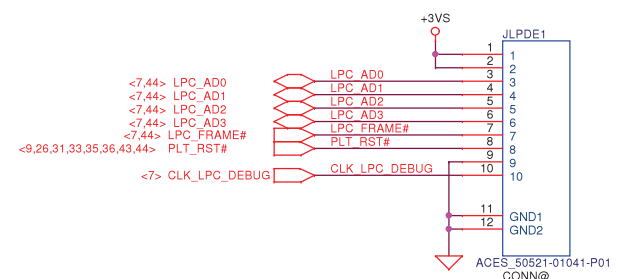
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Size	Document Number	LA-D311P		Rev	0.3
Date:	Friday, December 25, 2015	Sheet	18	of	51



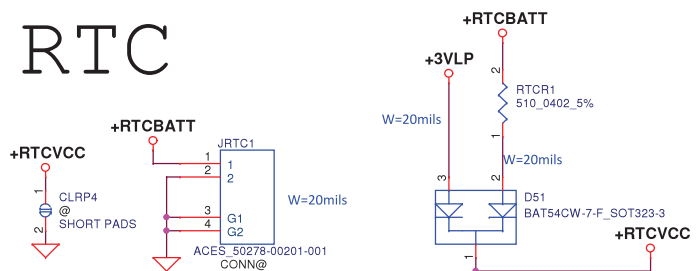
WIN debug



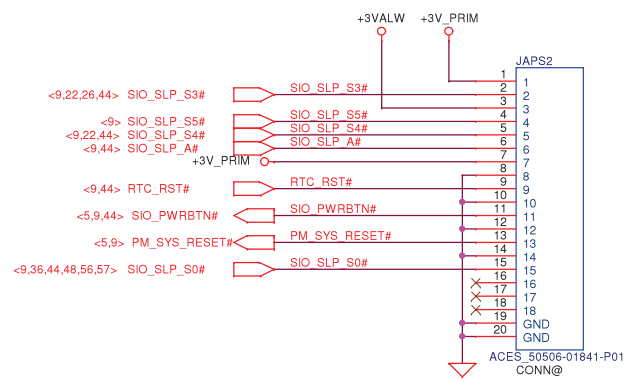
BIOS debug



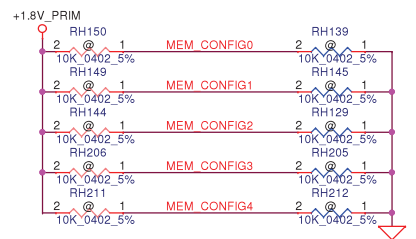
RTC



APS



DDR Memory Configuratio Type Strap pin

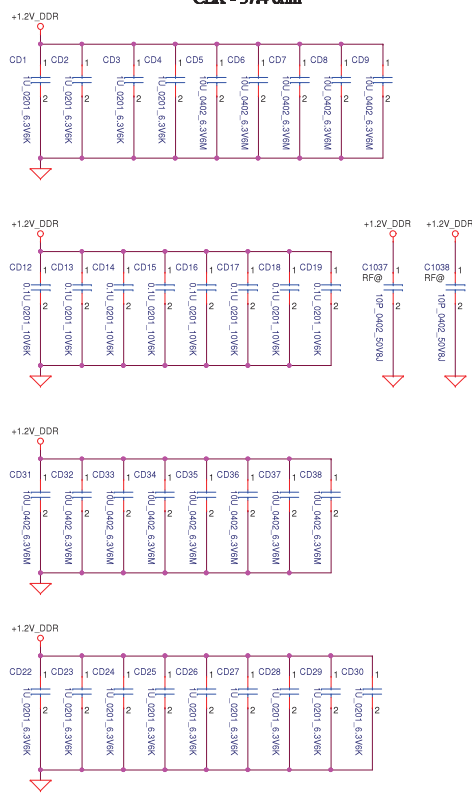
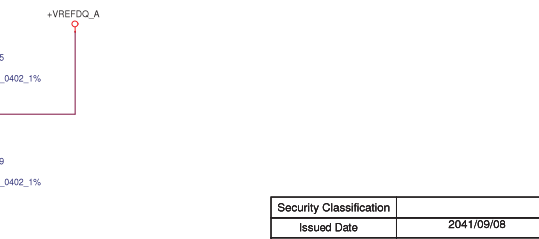
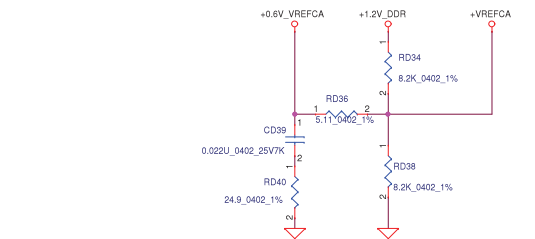


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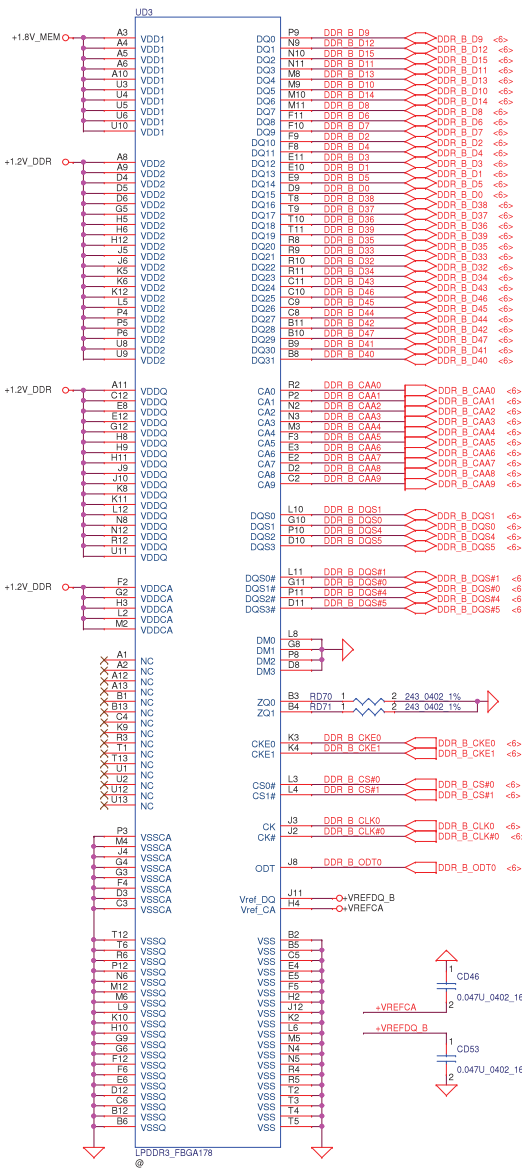
Pin Name	Micron 4GB SA00008PF0L	Micron 8GB SA00008Q10L	Micron 16GB SA00008QW0L	Hynix 4GB SA00008G60L	Hynix 8GB SA00008FJ0L	Hynix 16GB SA00008YT0L	Samsung 4GB SA00008PQ1L	Samsung 8GB SA00008QV1L	Samsung 16GB SA00008X11L
MEM_CONFIG0	0	1	0	1	0	1	0	1	0
MEM_CONFIG1	0	0	1	1	0	0	1	1	0
MEM_CONFIG2	0	0	0	0	1	1	1	1	0
MEM_CONFIG3	0	0	0	0	0	0	0	0	1
MEM_CONFIG4	0	0	0	0	0	0	0	0	0

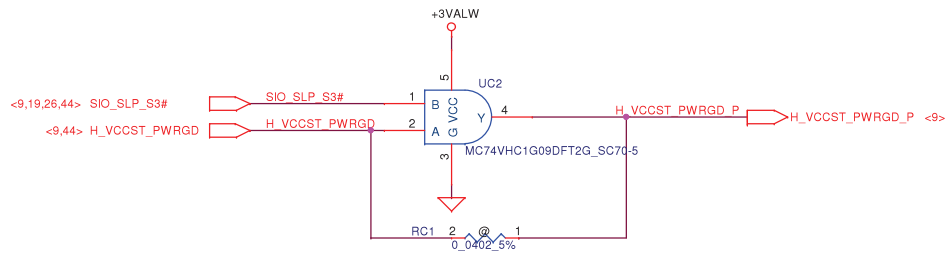
DRAM Option						DRAM Config Option					X76
						MEM_CONFIG0	MEM_CONFIG1	MEM_CONFIG2	MEM_CONFIG3	MEM_CONFIG4	
<b>Micron 4G/1866</b>						X76_M4G@ UD1 EDFA132A3MA-JD-F-R A3 SA00008PF1L	X76_M4G@ UD2 EDFA132A3MA-JD-F-R A3 SA00008PF1L	X76_M4G@ UD3 EDFA132A3MA-JD-F-R A3 SA00008PF1L	X76_M4G@ UD4 EDFA132A3MA-JD-F-R A3 SA00008PF1L	X76_M4G@ UD5 EDFA132A3MA-JD-F-R A3 SA00008PF1L	X7666031L03
<b>Micron 8G/1866</b>						X76_M8G@ UD1 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X76_M8G@ UD2 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X76_M8G@ UD3 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X76_M8G@ UD4 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X76_M8G@ UD5 EDFA232A2MA-JD-F-R A3 SA00008Q11L	X7666031L06
<b>Micron 16G/1866</b>						X76_M16G@ UD1 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X76_M16G@ UD2 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X76_M16G@ UD3 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X76_M16G@ UD4 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X76_M16G@ UD5 EDFA232A1MA-JD-F-R A3 SA00008QW1L	X7666031L09
<b>Hynix 4G/1866</b>						X76_H4G@ UD1 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X76_H4G@ UD2 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X76_H4G@ UD3 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X76_H4G@ UD4 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X76_H4G@ UD5 H9CCNNN8GTMLAR-NUD A3 SA00008G61L	X7666031L01
<b>Hynix 8G/1866</b>						X76_H8G@ UD1 H9CCNNNBTMLAR-NUD A3 SA00008FJ1L	X76_H8G@ UD2 H9CCNNNBTMLAR-NUD A3 SA00008FJ1L	X76_H8G@ UD3 H9CCNNNBTMLAR-NUD A3 SA00008FJ1L	X76_H8G@ UD4 H9CCNNNBTMLAR-NUD A3 SA00008FJ1L	X76_H8G@ UD5 H9CCNNNBTMLAR-NUD A3 SA00008FJ1L	X7666031L04
<b>Hynix 16G/1866</b>						X76_H16G@ UD1 H9CCNNNCLTMLAR-NUD A3 SA00008YT1L	X76_H16G@ UD2 H9CCNNNCLTMLAR-NUD A3 SA00008YT1L	X76_H16G@ UD3 H9CCNNNCLTMLAR-NUD A3 SA00008YT1L	X76_H16G@ UD4 H9CCNNNCLTMLAR-NUD A3 SA00008YT1L	X76_H16G@ UD5 H9CCNNNCLTMLAR-NUD A3 SA00008YT1L	X7666031L07
<b>Samsung 4G/1866</b>						X76_S4G@ UD1 K4EBE304EE-EGCF A31 SA00008PQ1L	X76_S4G@ UD2 K4EBE304EE-EGCF A31 SA00008PQ1L	X76_S4G@ UD3 K4EBE304EE-EGCF A31 SA00008PQ1L	X76_S4G@ UD4 K4EBE304EE-EGCF A31 SA00008PQ1L	X76_S4G@ UD5 K4EBE304EE-EGCF A31 SA00008PQ1L	X7666031L02
<b>Samsung 8G/1866</b>						X76_S8G@ UD1 K4EBE304EB-EGCF A31 SA00008QV1L	X76_S8G@ UD2 K4EBE304EB-EGCF A31 SA00008QV1L	X76_S8G@ UD3 K4EBE304EB-EGCF A31 SA00008QV1L	X76_S8G@ UD4 K4EBE304EB-EGCF A31 SA00008QV1L	X76_S8G@ UD5 K4EBE304EB-EGCF A31 SA00008QV1L	X7666031L05
<b>Samsung 16G/1866</b>						X76_S16G@ UD1 K4EBE304EB-EGCF A31 SA00008X11L	X76_S16G@ UD2 K4EBE304EB-EGCF A31 SA00008X11L	X76_S16G@ UD3 K4EBE304EB-EGCF A31 SA00008X11L	X76_S16G@ UD4 K4EBE304EB-EGCF A31 SA00008X11L	X76_S16G@ UD5 K4EBE304EB-EGCF A31 SA00008X11L	X7666031L08

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						Size		Document Number		Rev	
						LA-D311P		0.3			
						Date:		Friday, December 25, 2015		Sheet 19 of 51	

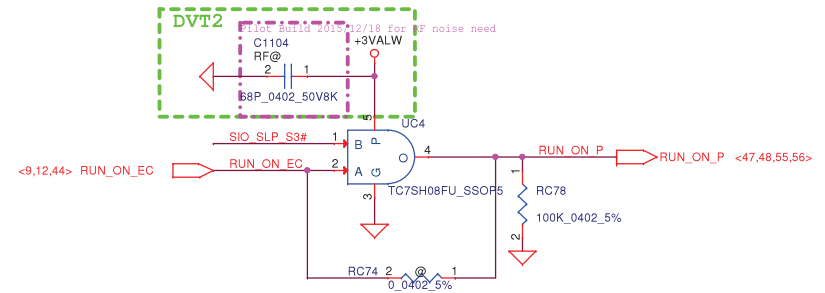


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			Date	2016-06-16
			Drawn	99 of 61

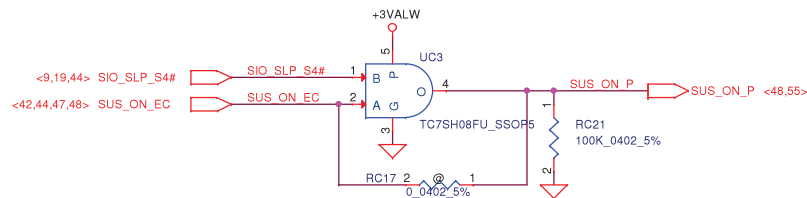




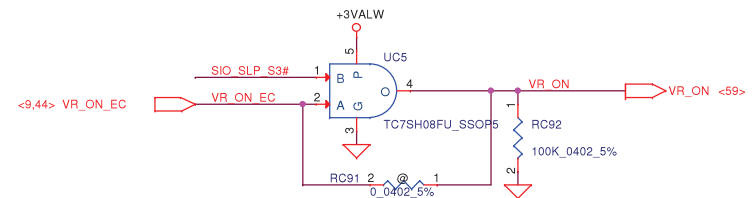
Change CPU VCCST\_PWRGD enable from EC & PCH  
H\_VCCST\_PWRGD (3.3V), H\_VCCST\_PWRGD\_P (1.0V)  
If need to mount RC1, need to add level shift.



Change VCCIO & VCCSTG power enable from EC & PCH



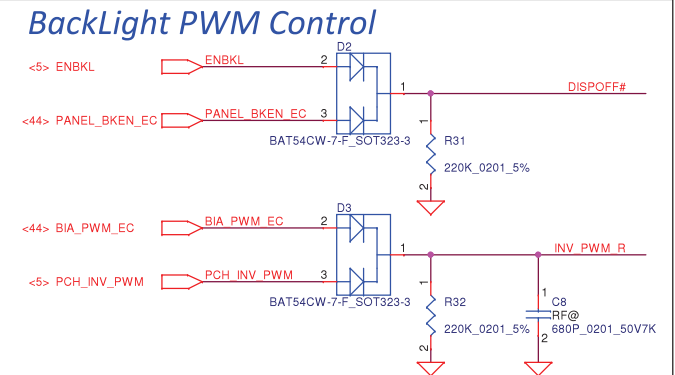
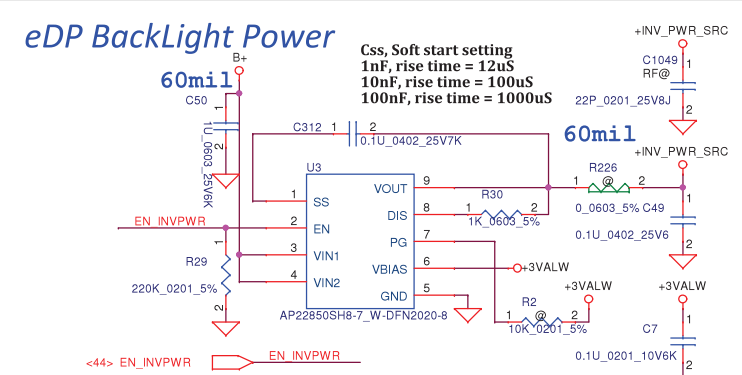
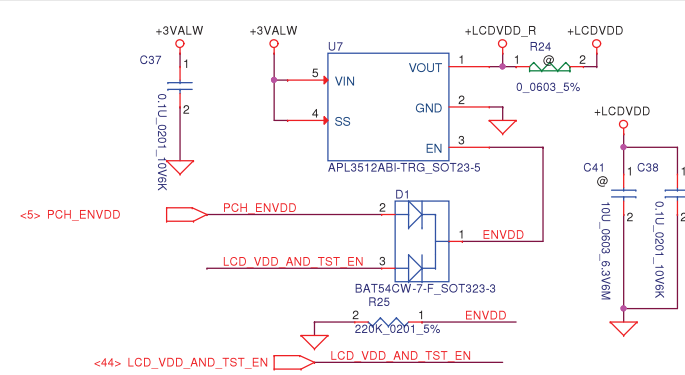
Change VCCST & 1.2\_VR power enable from EC & PCH



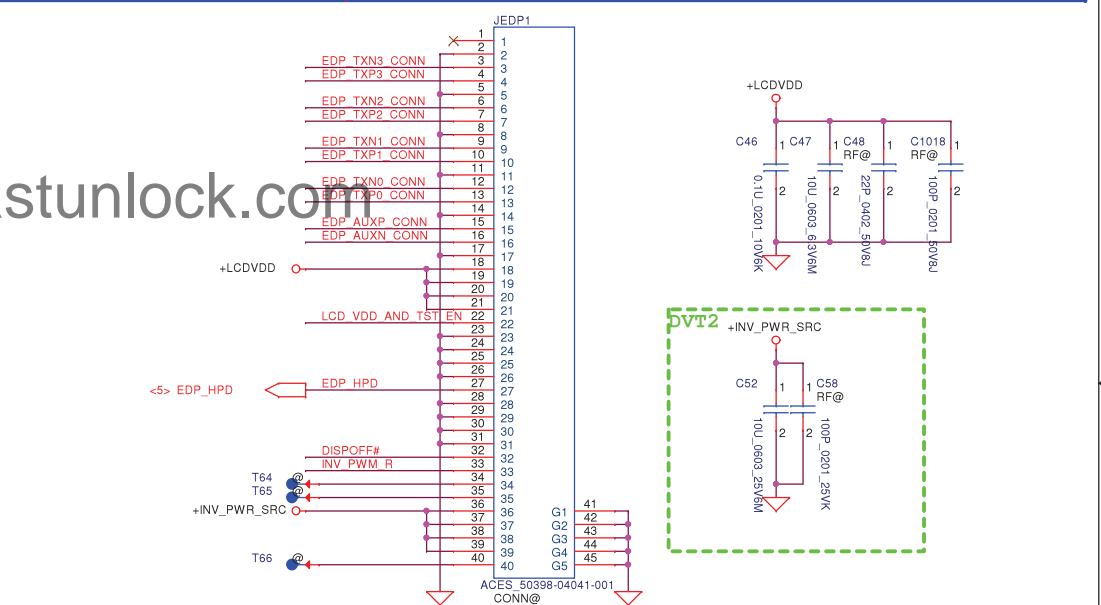
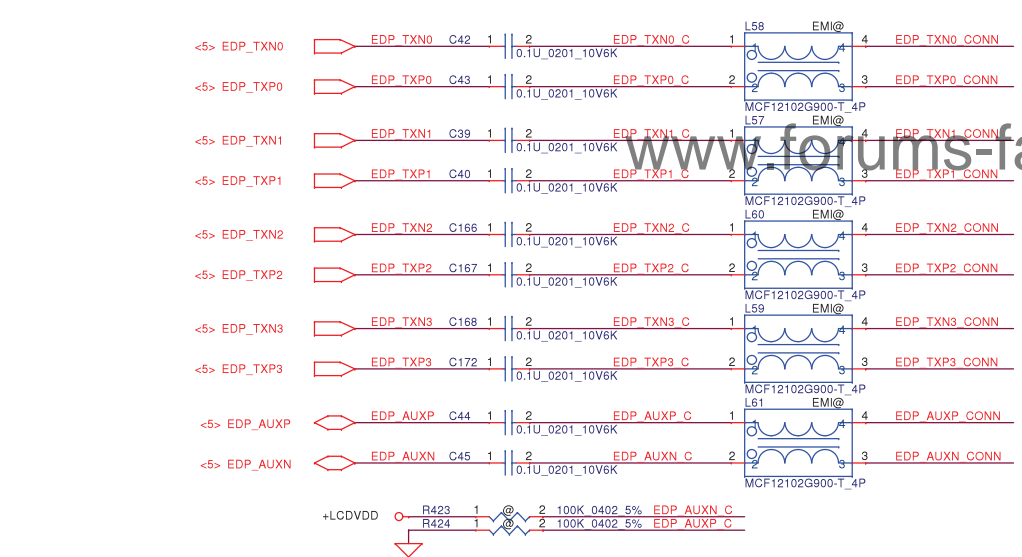
Change VCORE power enable from EC & PCH

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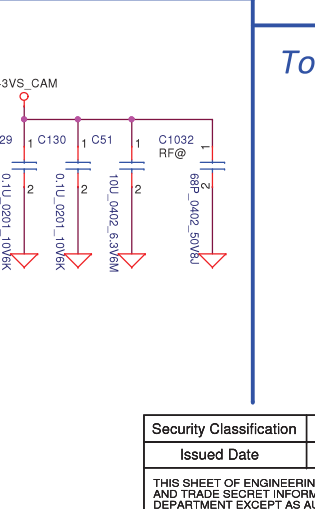
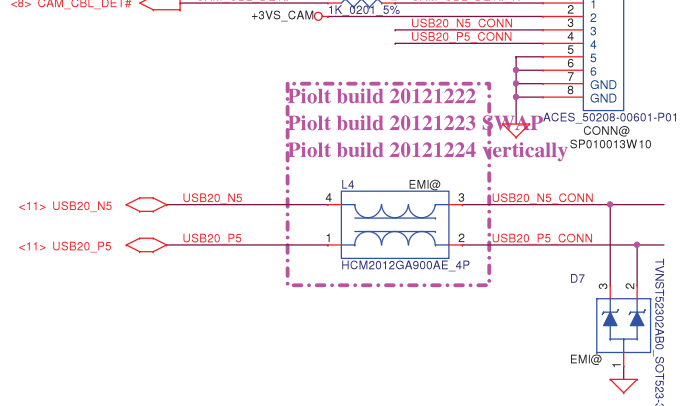
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Size	Document Number	Rev			0.3
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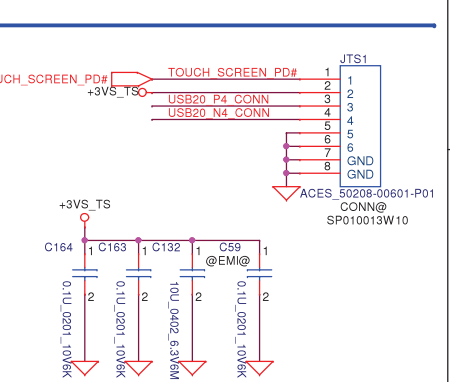
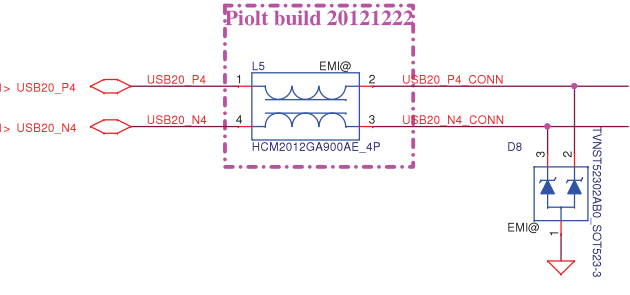
# eDP Conn



# CAM



# Touch Screen



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+3VS RV15 1 2 4.7K 0201 5% DP\_CFG0

Chip operational mode configuration;  
Internal pull down at ~150K?, 3.3V I/O.

L: Control switching mode (default)  
H: Automatic switching mode

+3VS RV23 1 2 4.7K 0201 5% P10

Automatic EQ disable;  
Internal pull down at ~150K?, 3.3V I/O

L: Automatic EQ enable (default)  
H: Automatic EQ disable

+3VS RV27 1 2 4.7K 0201 5% P11

Auto test enable;  
Internal pull down at ~150K?, 3.3V I/O.  
L: Auto test disable & input offset cancellation enable (default)  
H: Auto test enable & input offset cancellation enable  
M: Auto test disable & input offset cancellation disable

+3VS RV16 1 2 4.7K 0201 5% UV2\_PC10

RV17 1 2 4.7K 0201 5%

+3VS RV18 1 2 4.7K 0201 5% UV2\_PC20

RV19 1 2 4.7K 0201 5%

AUX interception disable for Port y (y=1,2)  
Internal pull down at ~150K?, 3.3V I/O.

L: AUX interception enable, driver configuration is set by link training (default)  
H: AUX interception disable, driver output with fixed 800mv and 0dB  
M: AUX interception disable, driver output with fixed 400mv and 0dB

+3VS RV20 1 2 4.7K 0201 5% UV2\_PC11

RV21 1 2 4.7K 0201 5%

+3VS RV22 1 2 4.7K 0201 5% UV2\_PC21

RV24 1 2 4.7K 0201 5%

Output swing adjustment for Port y (y=1,2).  
Internal pull down at ~150K?, 3.3V I/O.

L: default  
H: +20%  
M: -16.7%

+3VS RV25 1 2 4.7K 0201 5% PEQ

RV26 1 2 4.7K 0201 5%

Programmable input equalization levels; Internal pull down at ~150K?, 3.3V I/O.

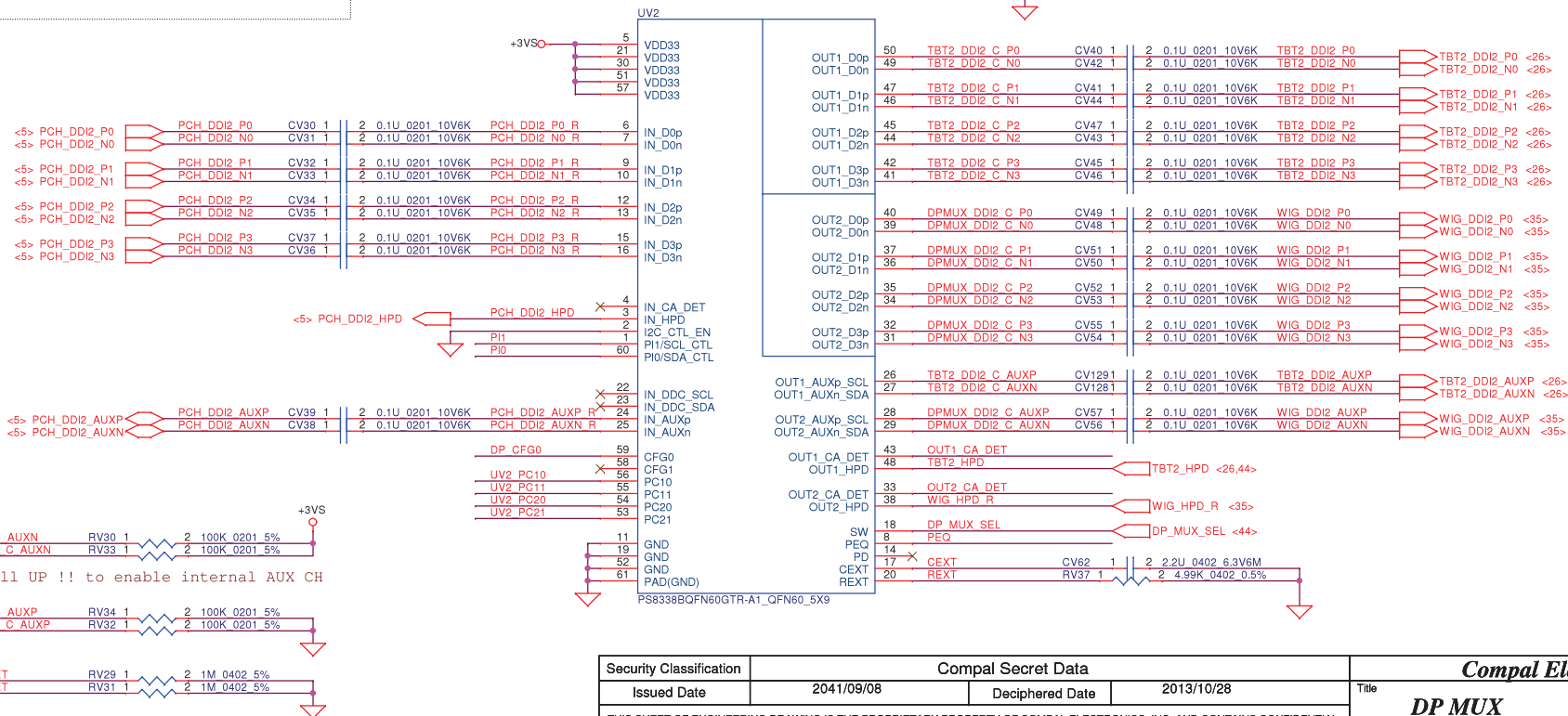
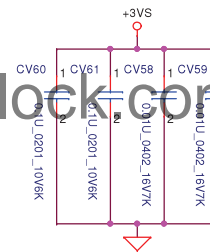
L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2  
H: HEQ, compensate channel loss up to 14.5dB @ HBR2  
M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

## DP\_MUX\_SEL pin

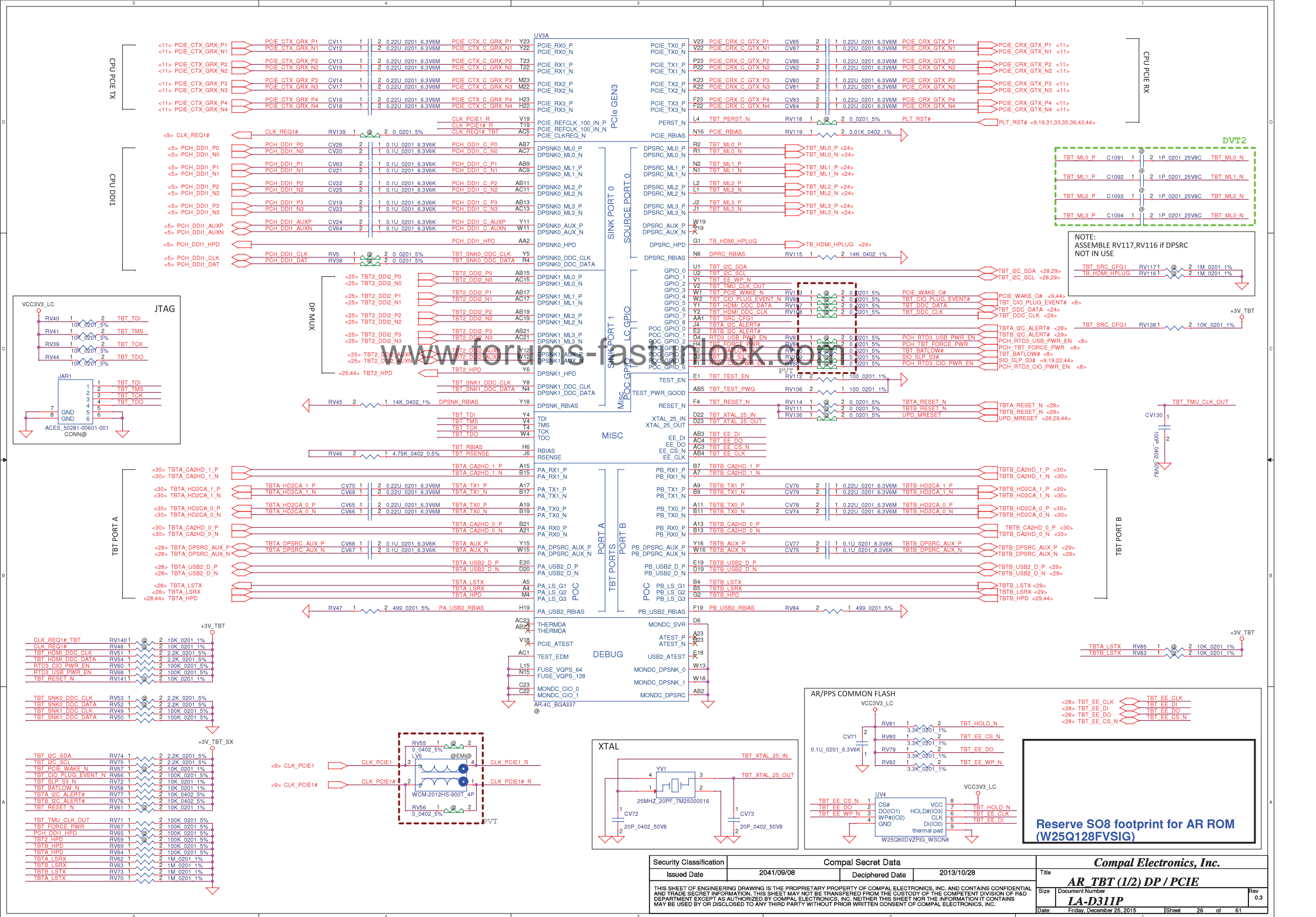
Port switching control or priority configuration;  
Internal pull down at ~150K?, 3.3V I/O.

L: Port1 is selected or with higher priority (default)  
H: Port2 is selected or with higher priority

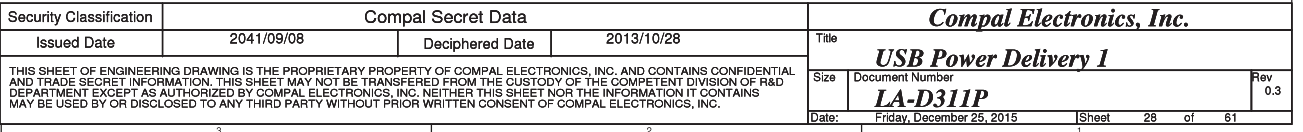
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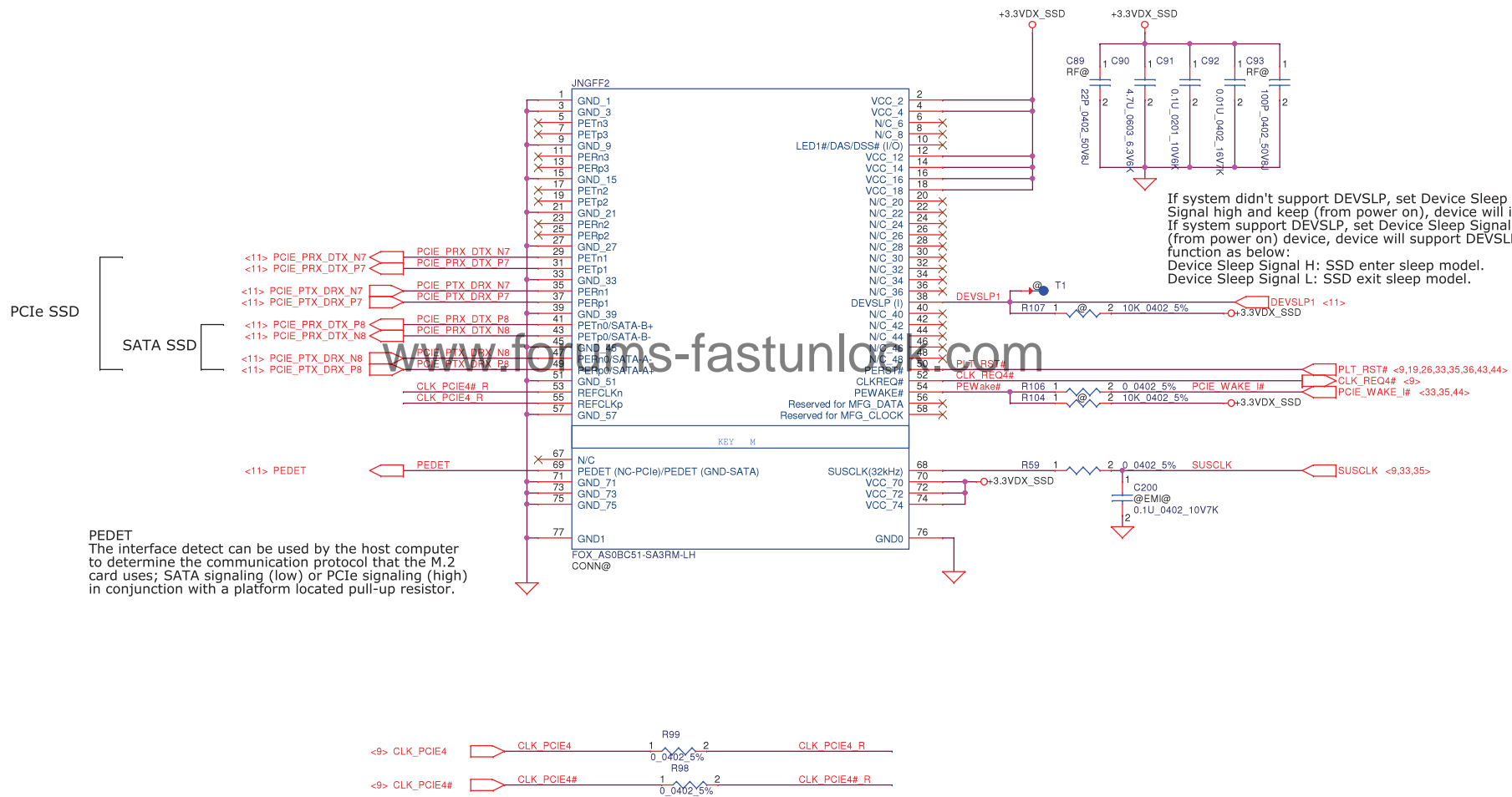








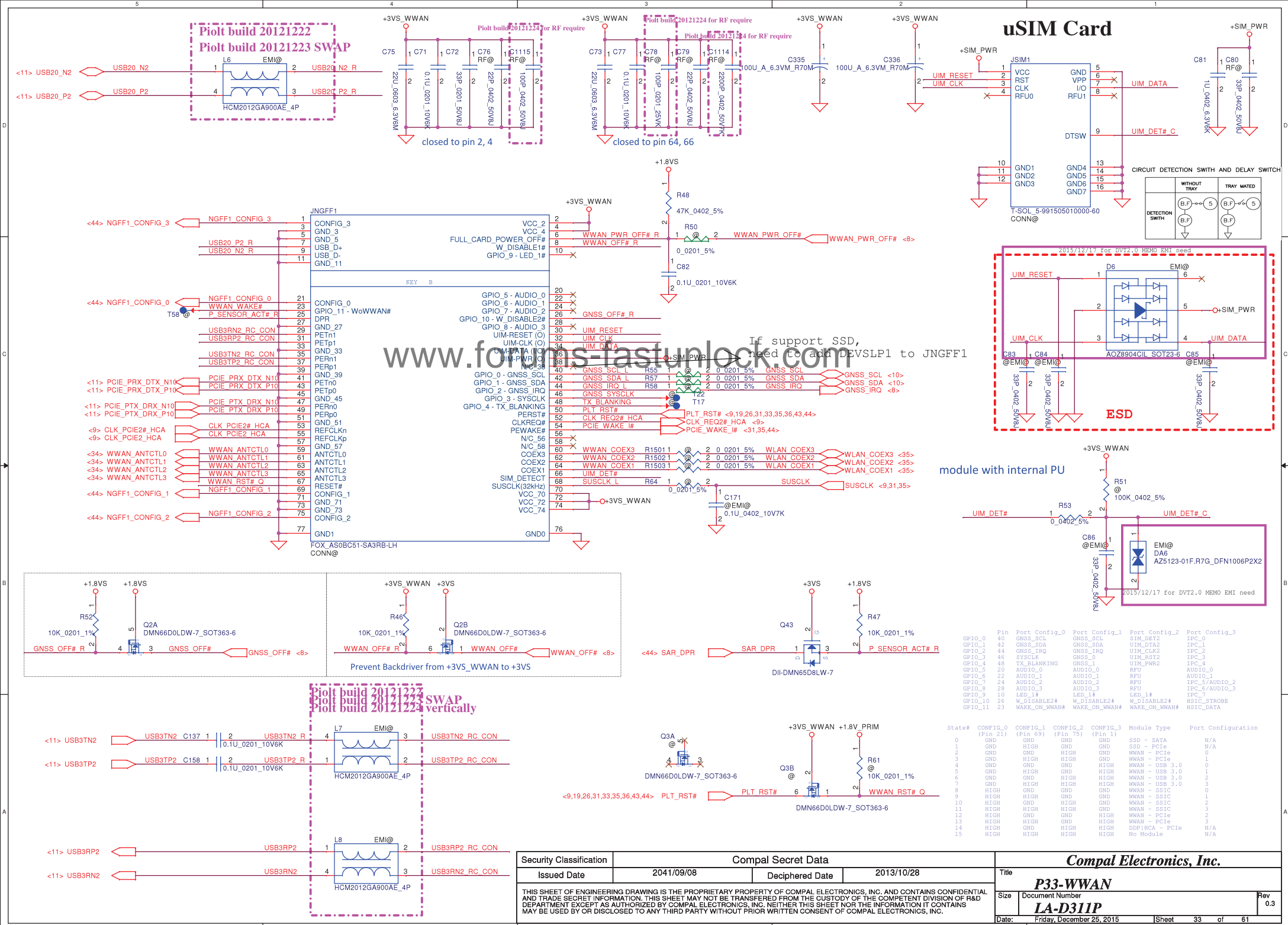
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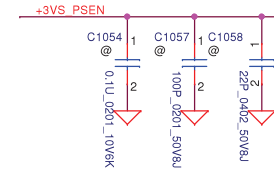
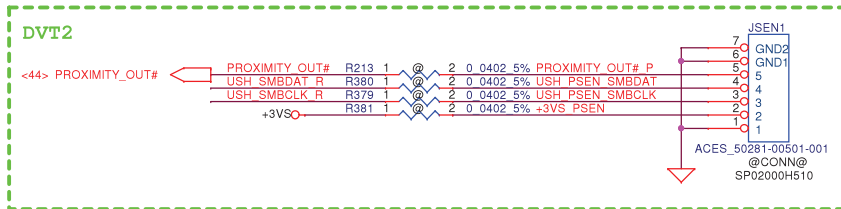
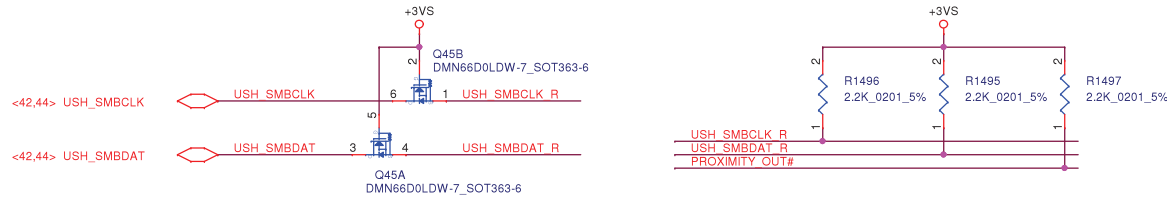
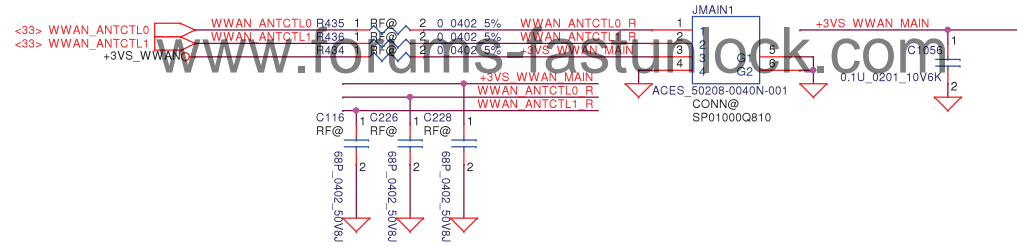
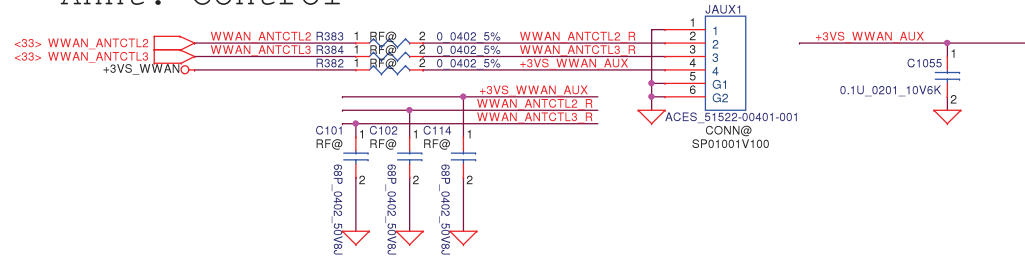
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Issued Date	2041/09/08	Deciphered Date	2013/10/28	SATA SSD	
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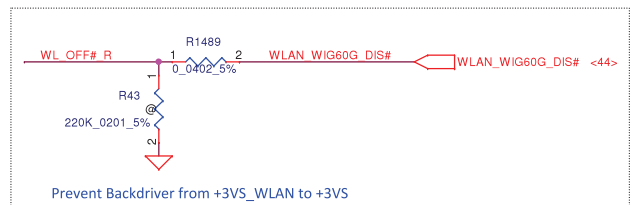
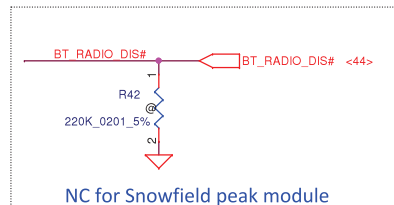
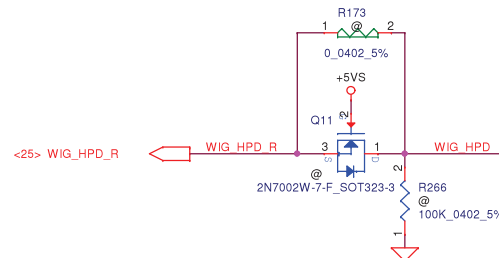
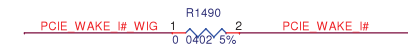
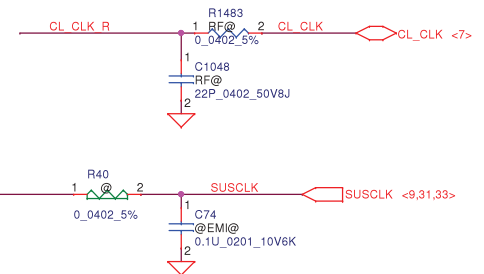
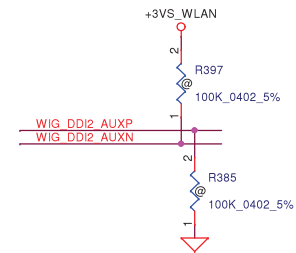
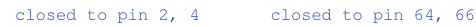


# Annt. Control



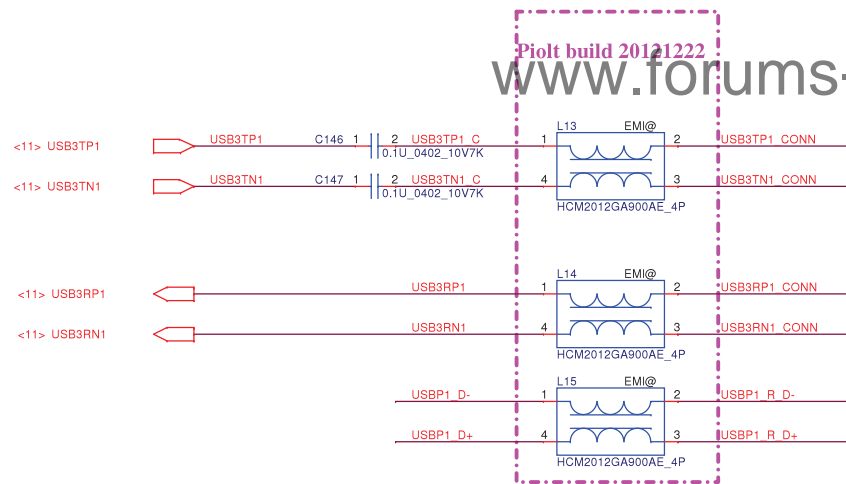
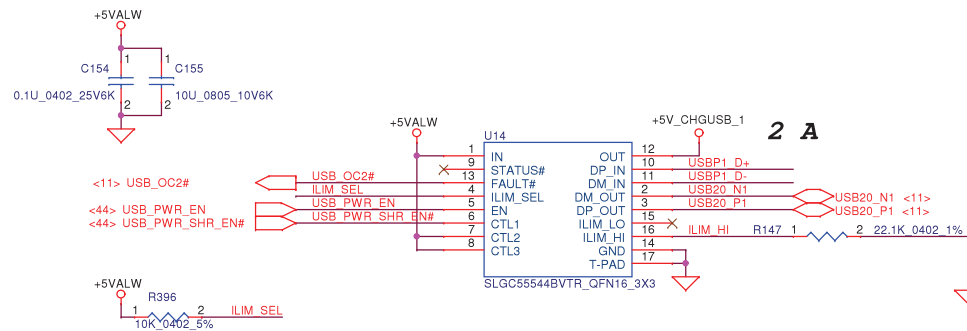
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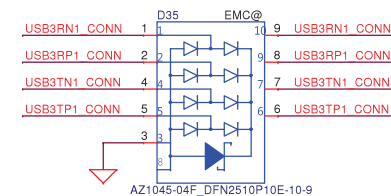
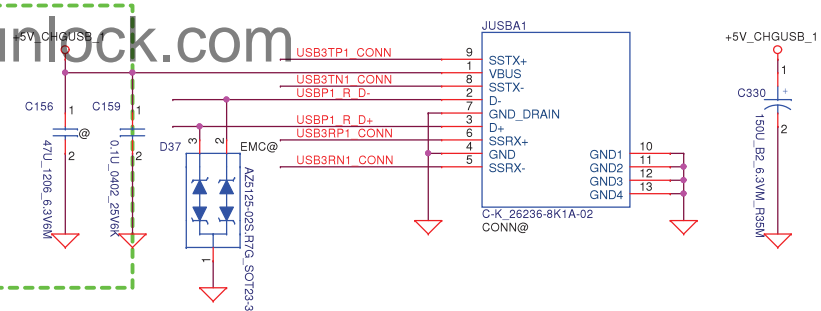


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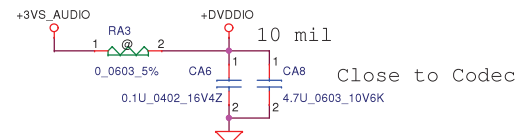
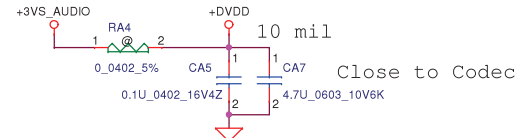
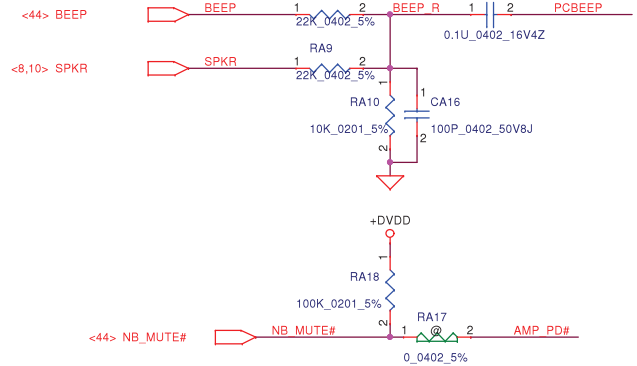
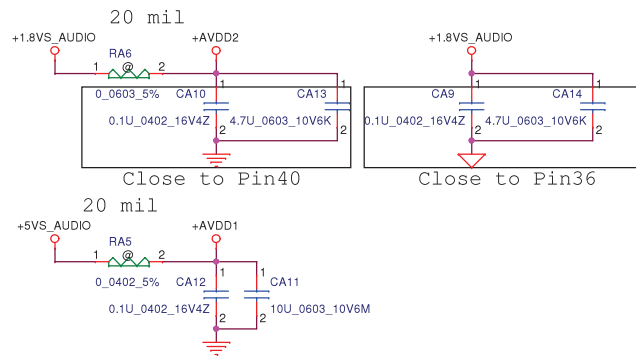
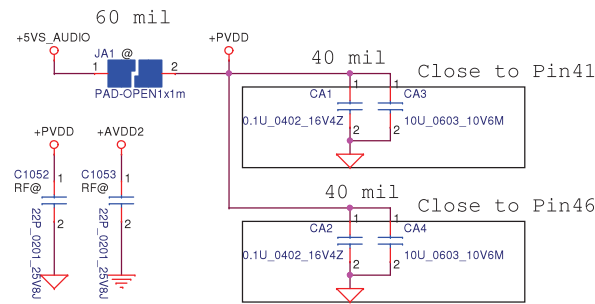




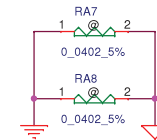
DVT2



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<8> HDA\_BITCLK\_AUDIO  
<8> HDA\_SDOUT\_AUDIO  
<8> HDA\_SDIN0

HDA\_SYNC\_AUDIO  
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HDA\_SDOUT\_AUDIO  
HDA\_SDIN0

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<46> DMIC\_CLK\_CODECD

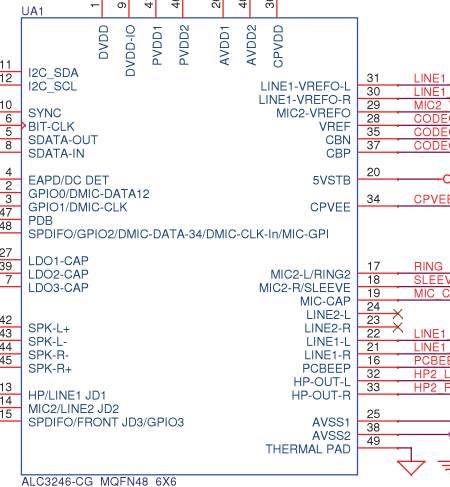
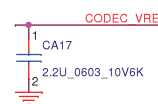
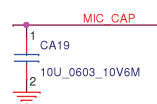
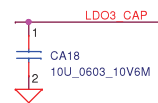
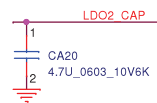
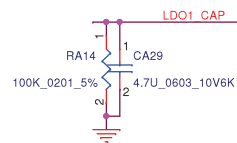
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DMIC\_CLK\_CODECD

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<39> SPK\_OUT\_L-  
<39> SPK\_OUT\_R+  
<39> SPK\_OUT\_R-

SPK\_OUT\_L+  
SPK\_OUT\_L-  
SPK\_OUT\_R+  
SPK\_OUT\_R-

<39> JACK\_DET#

JACK\_DET#



LINE1\_VREF0\_L  
LINE1\_VREF0\_R  
MIC2\_VREF0  
VREF  
CBN  
CODEC\_CBP  
5VSTB  
CPVEE  
RING  
SLEEVE  
MIC\_CAP  
LINE2\_L  
LINE2\_R  
LINE1\_L  
LINE1\_R  
PCBEEP  
HP2\_L  
HP2\_R  
AVSS1  
AVSS2  
THERMAL\_PAD

HDA\_BITCLK\_AUDIO  
CA33  
@EMC@  
10P\_0402\_50V8J

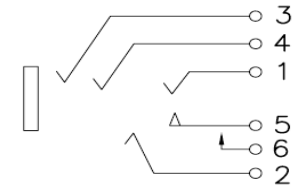
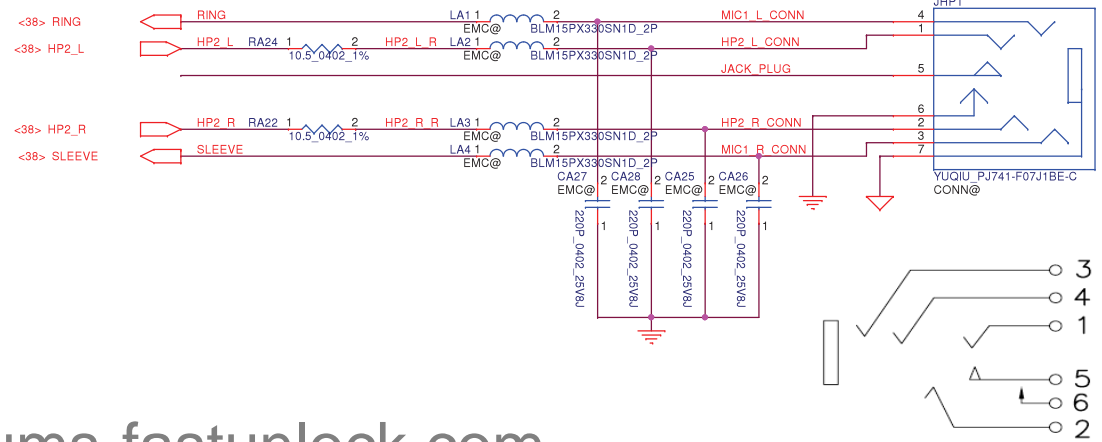
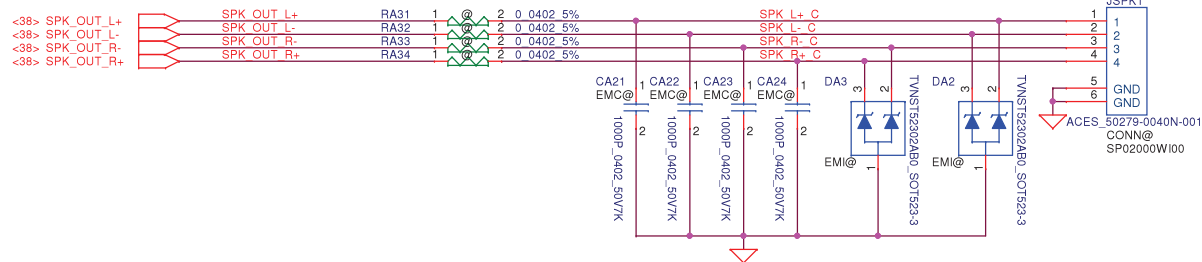
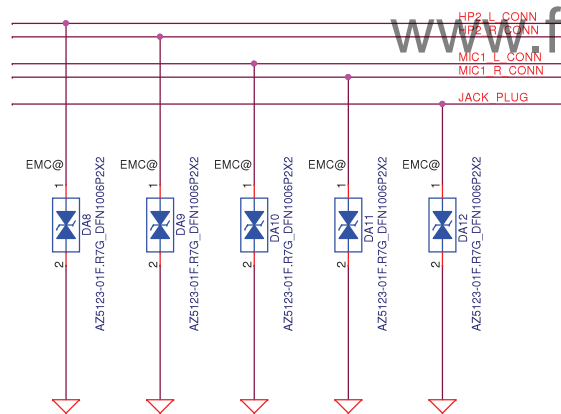
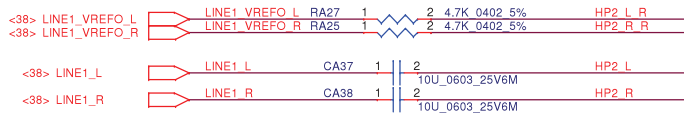
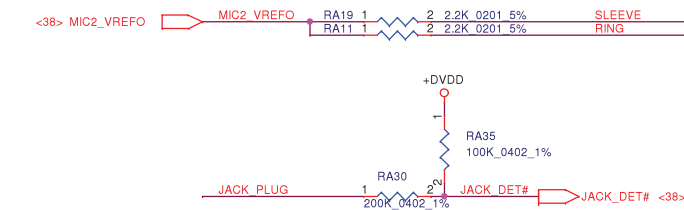
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HDA\_SYNC\_AUDIO  
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DMIC\_DAT\_CODECD  
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EMC@  
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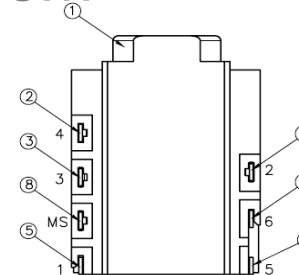
HDA\_SDOUT\_AUDIO  
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EMC@  
10P\_0402\_50V8J

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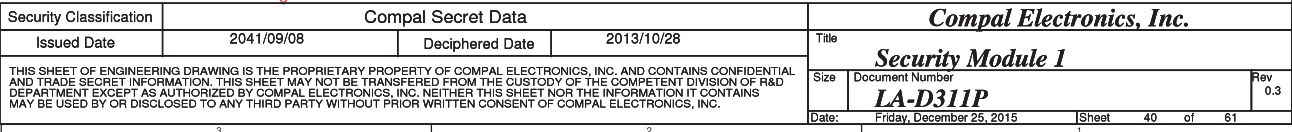


## SCHEMATIC

NO.	PART NAME	TER'NO.
10	SEPARATOR	
9	MYLAR	
8	SHIELD	
7	BREAK TERMINAL	6
6	TRANSFER TERMINAL	5
5	TIP TERMINAL	1
4	RING B TERMINAL	2
3	RING A TERMINAL	3
2	EARTH TERMINAL	4
1	HOUSING	

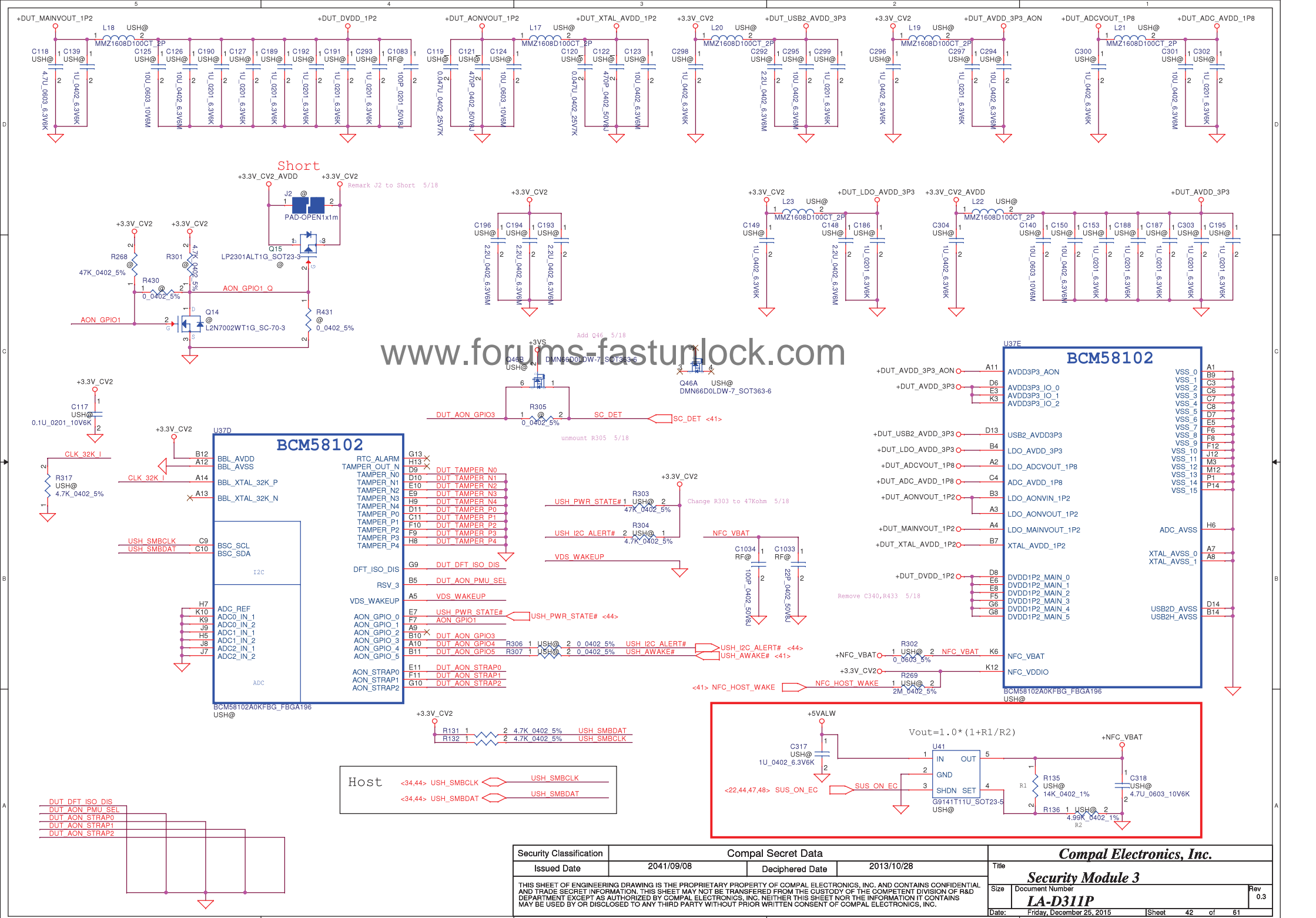


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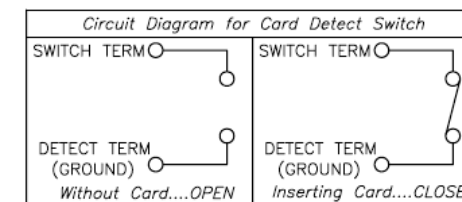
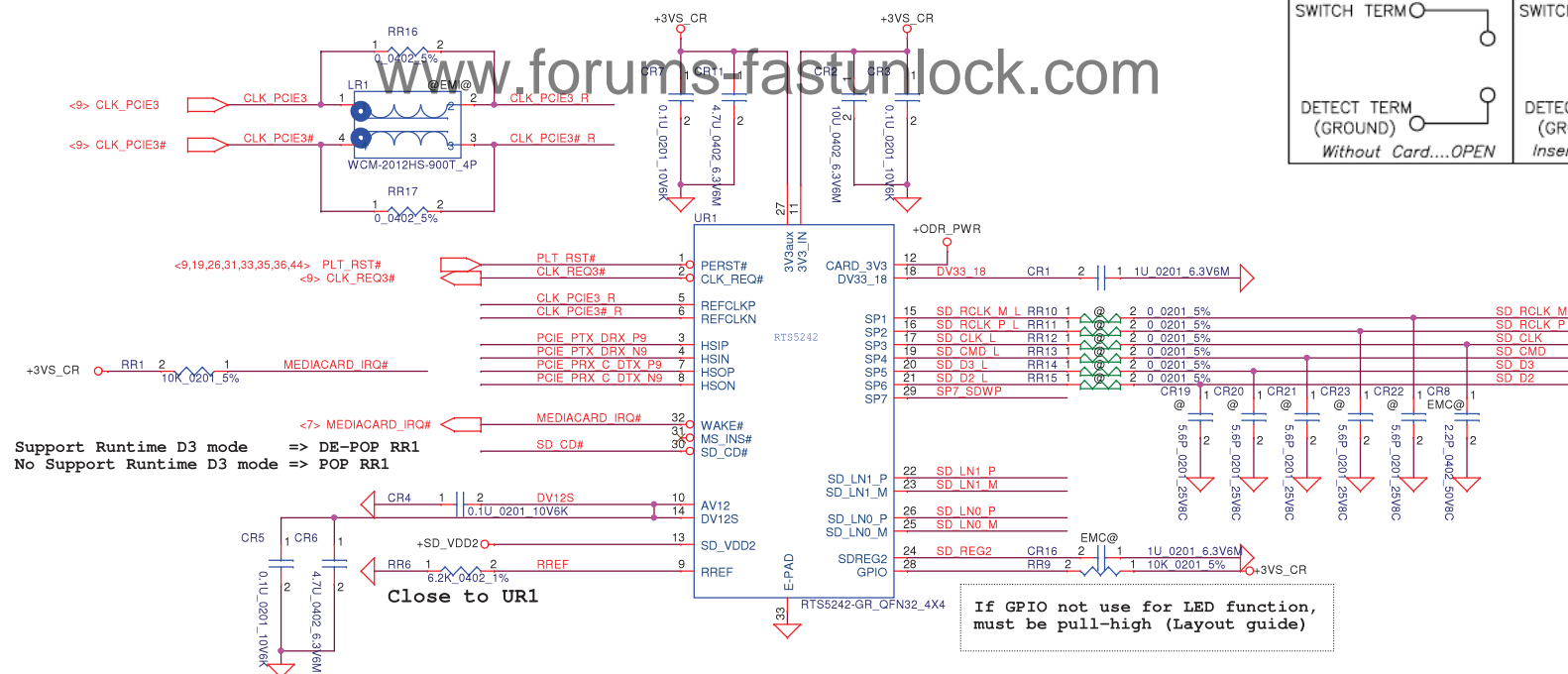
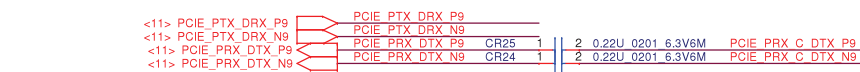
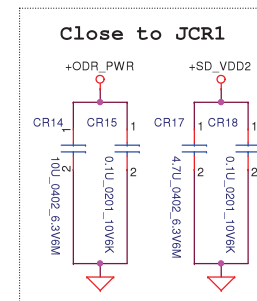
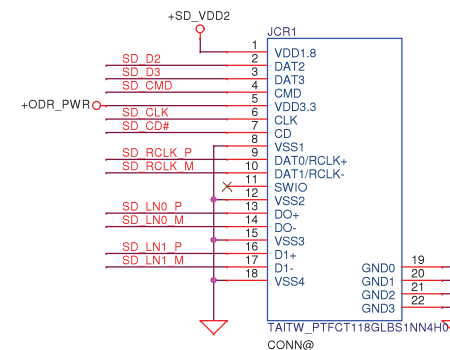
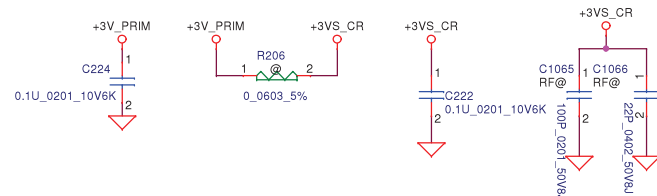




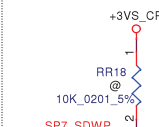
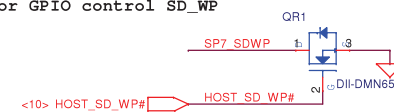


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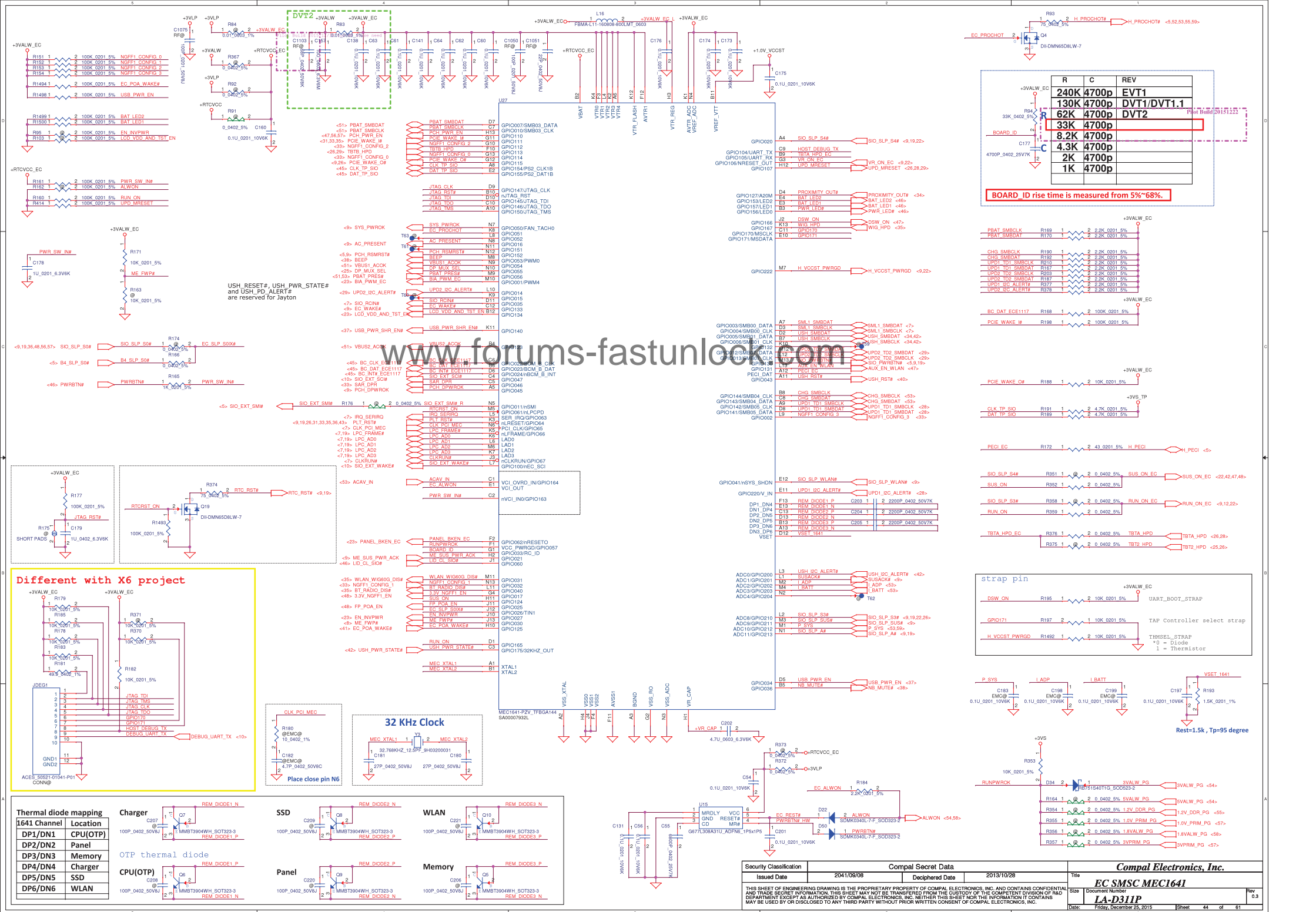
## Card Reader

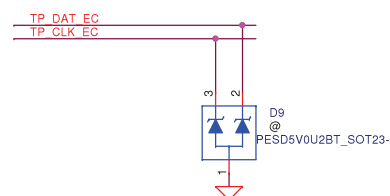
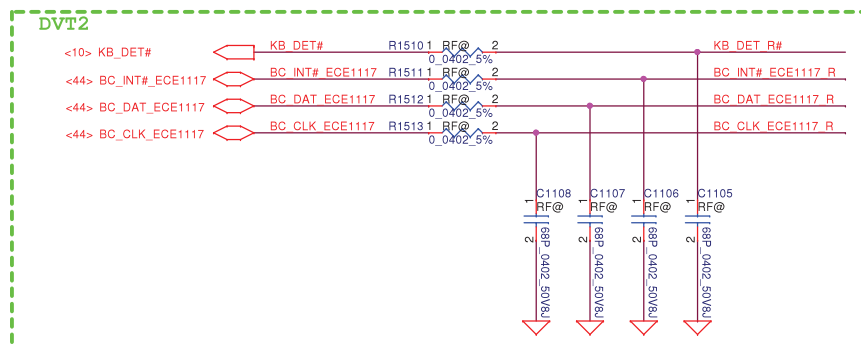
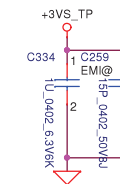
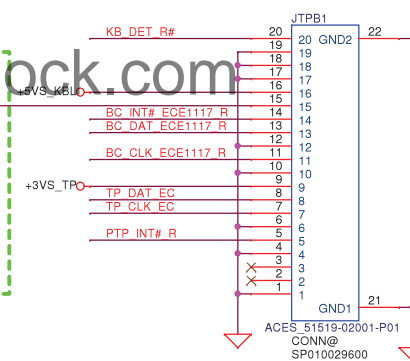
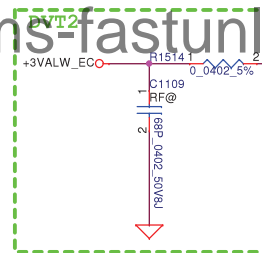
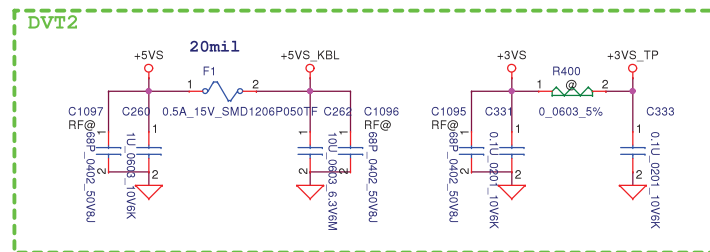
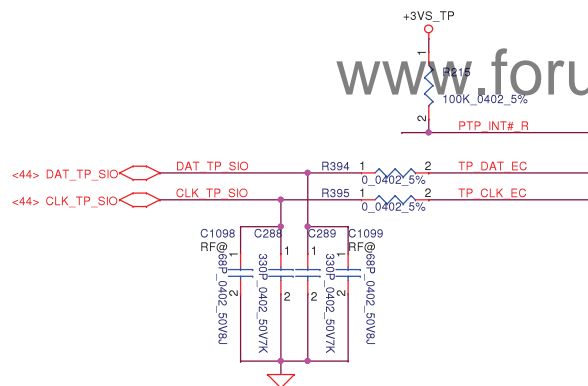


- 1) Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2) Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
  - Bulk capacitor for Card\_3V3 place closed to flash card socket.
  - Bulk capacitor for 3V3\_IN / 3V3aux / DV12S place closed to RTS5242 chip.
- 3) Keep damping resistor (ex, for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4) Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



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				Size Document Number	
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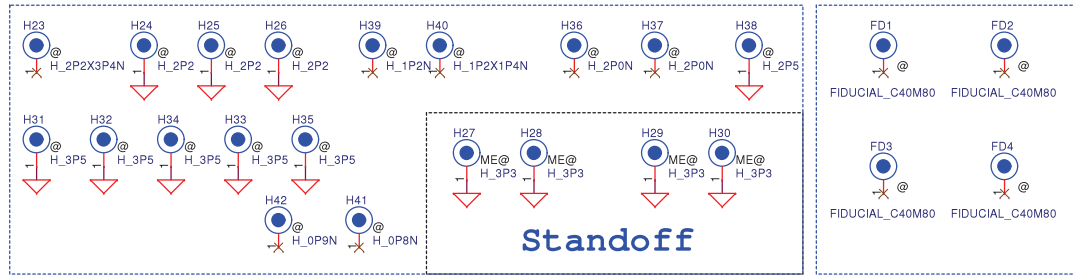




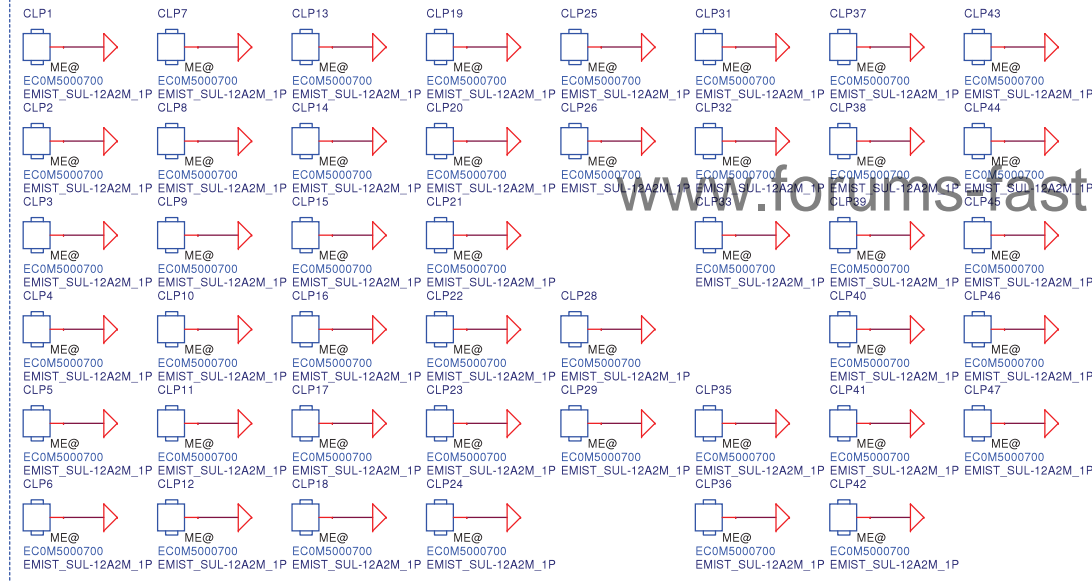
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2041/09/08	Deciphered Date	2013/10/28	Title	TouchPAD
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				Date	Friday, December 25, 2015
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				Rev	0.3



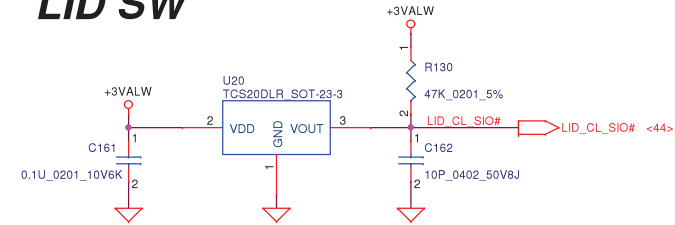
# Screw Hole



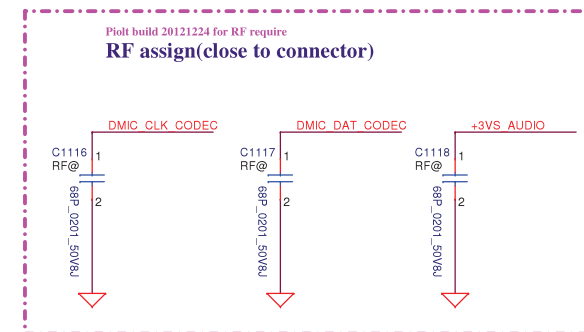
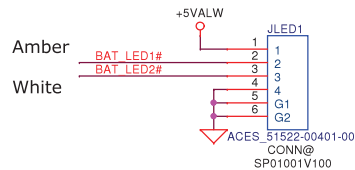
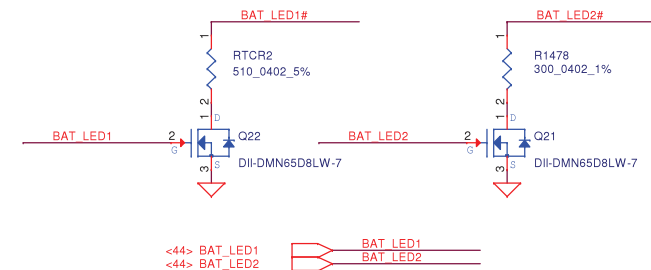
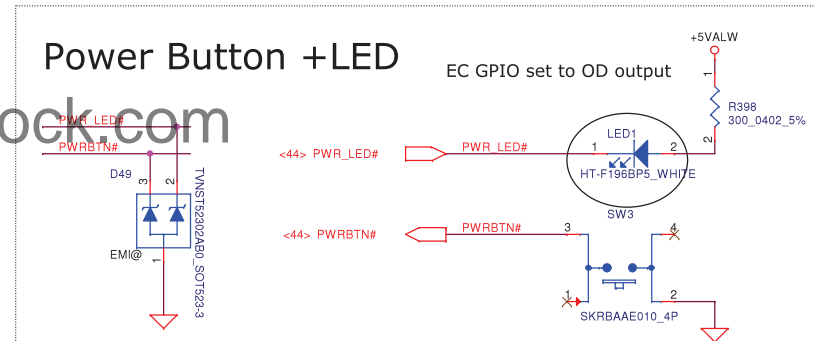
## CLIP. \*44



## LID SW

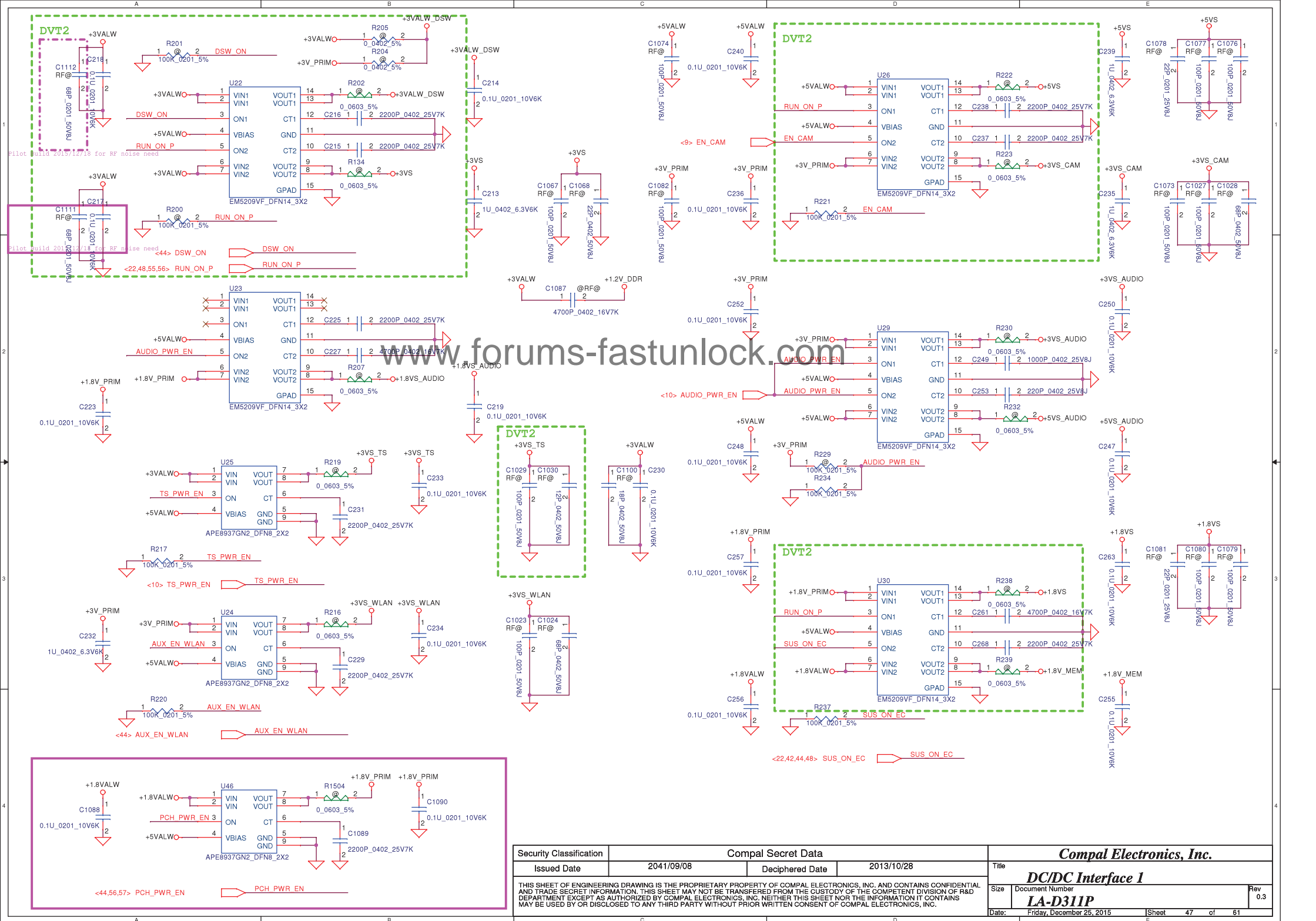


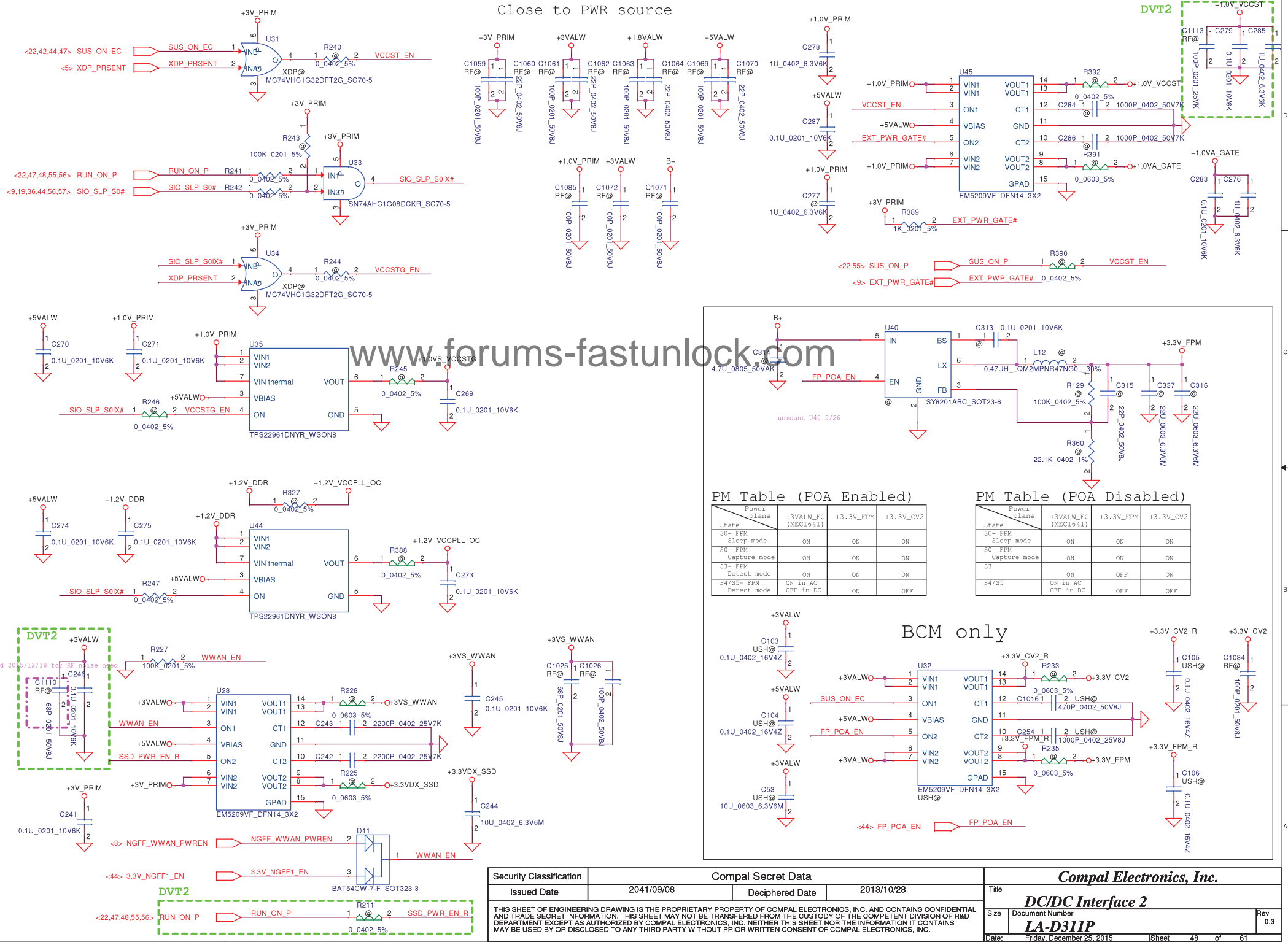
## Power Button +LED

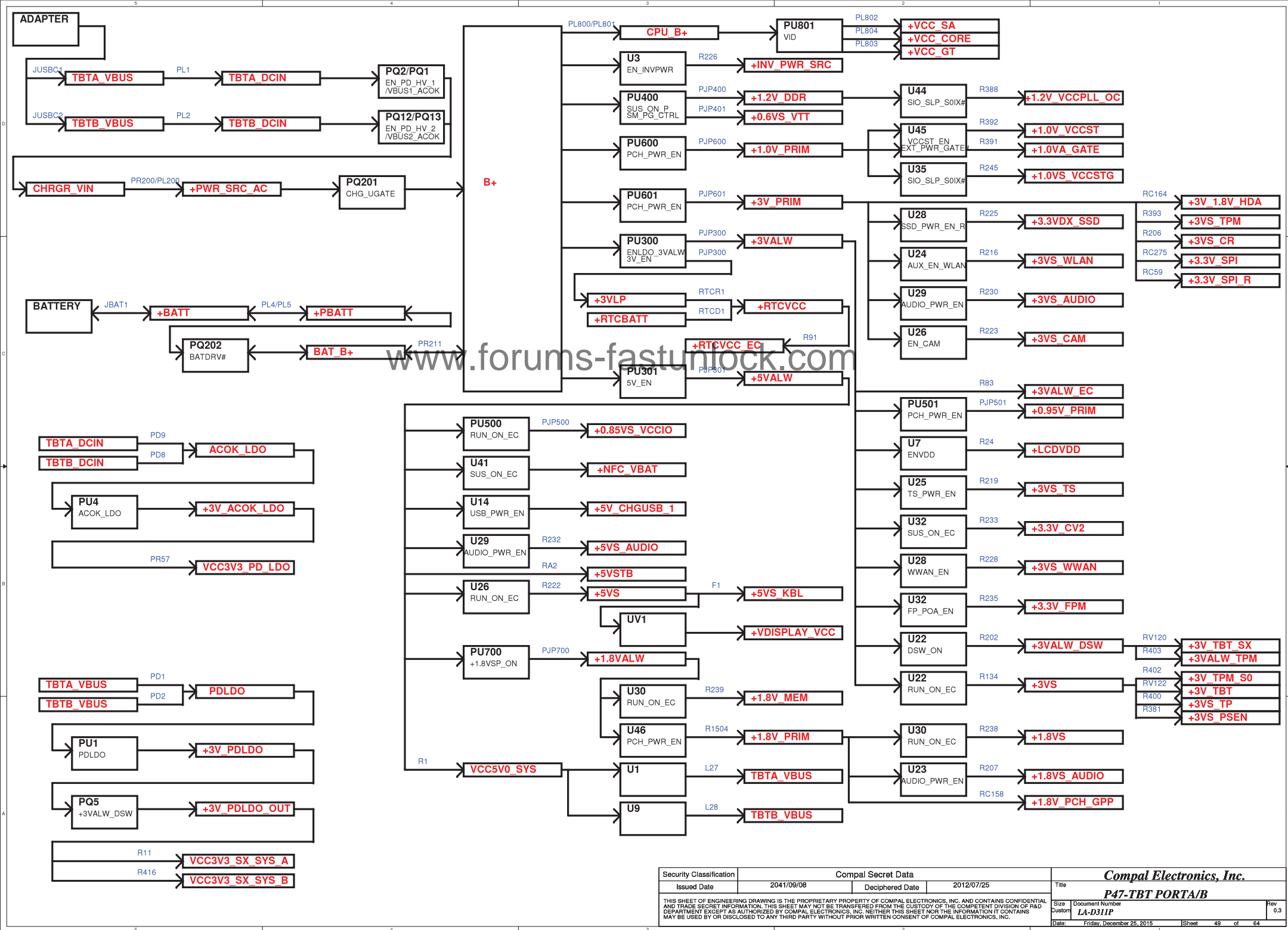


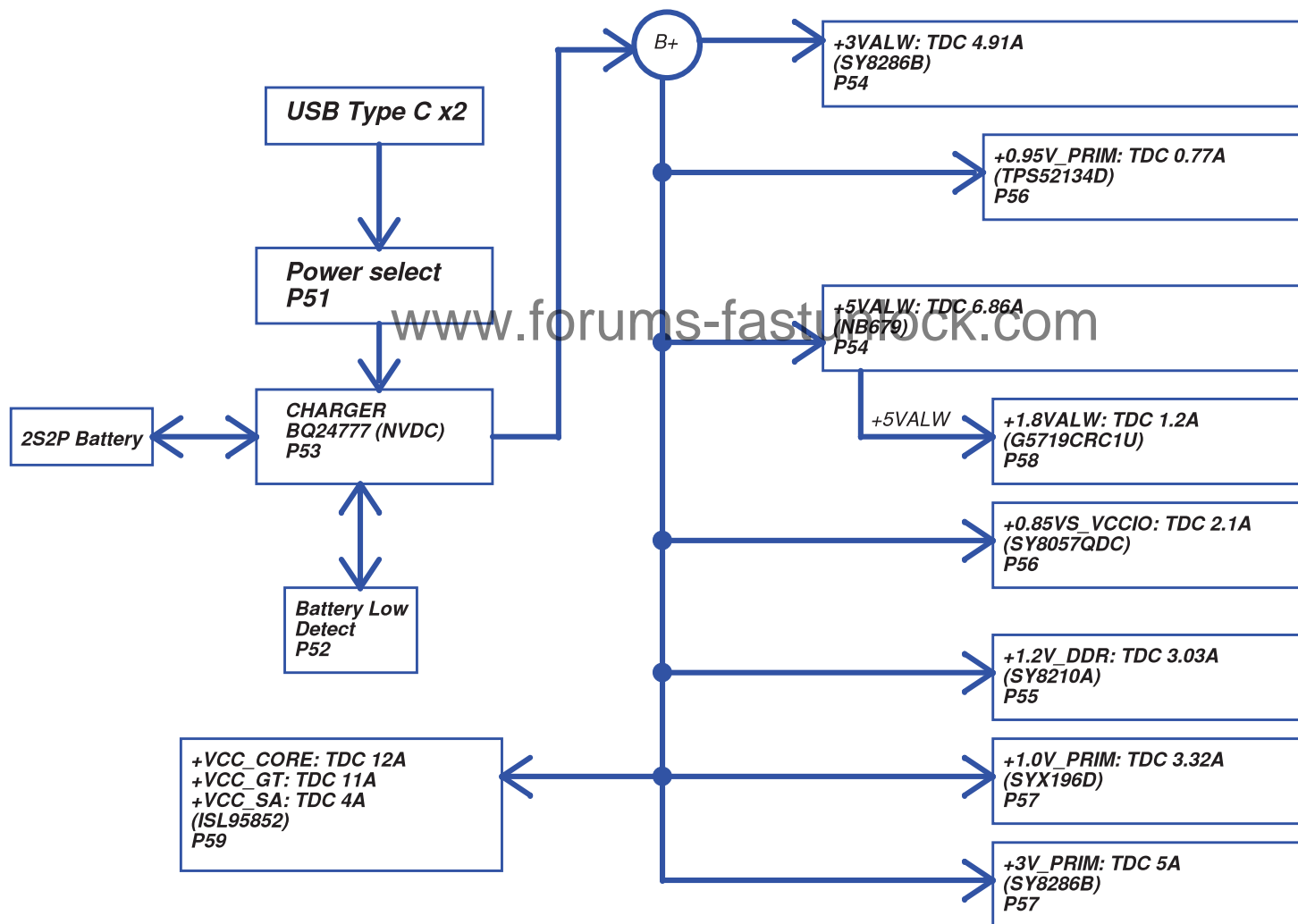
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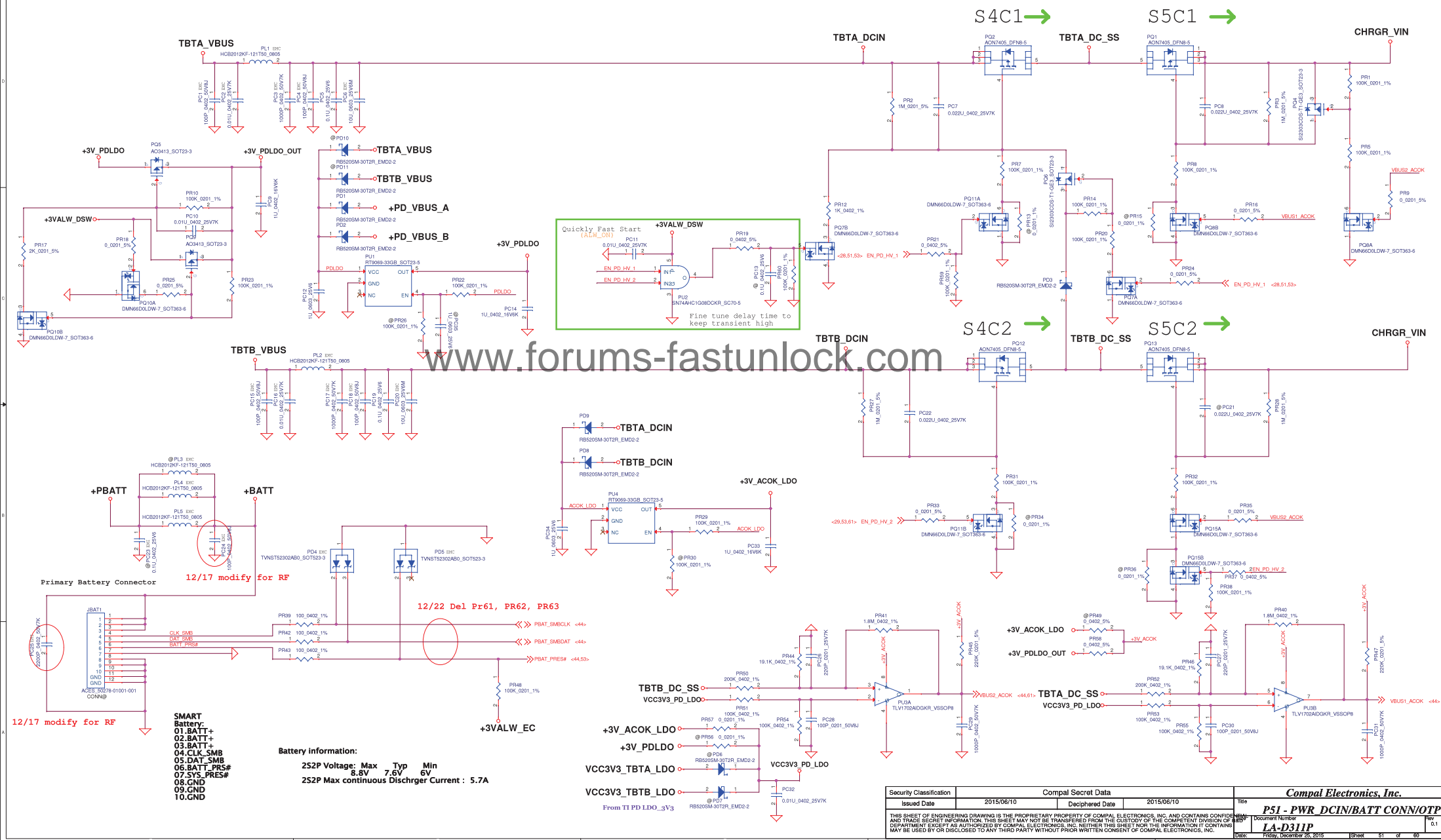








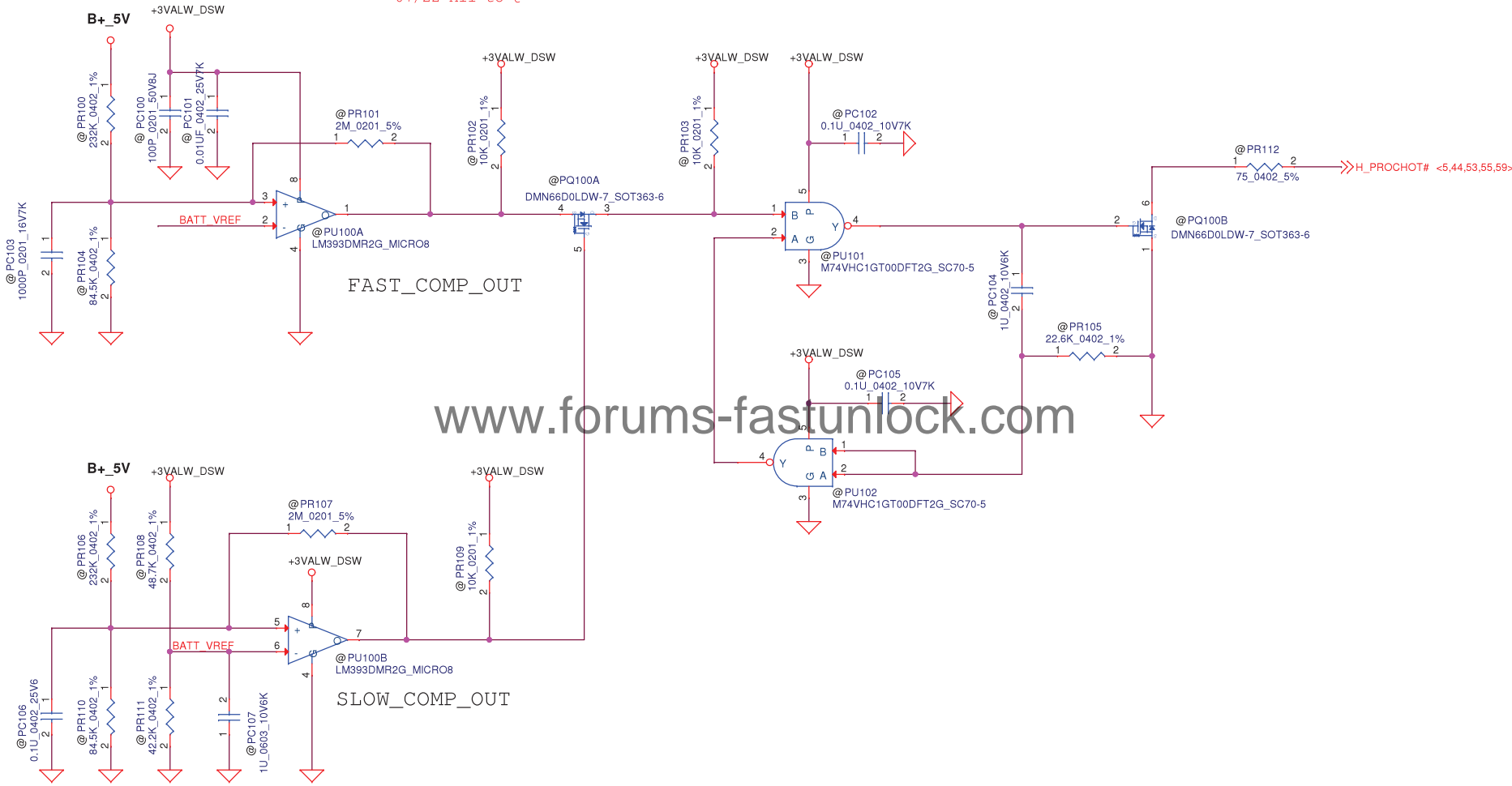






BATT low voltage detect

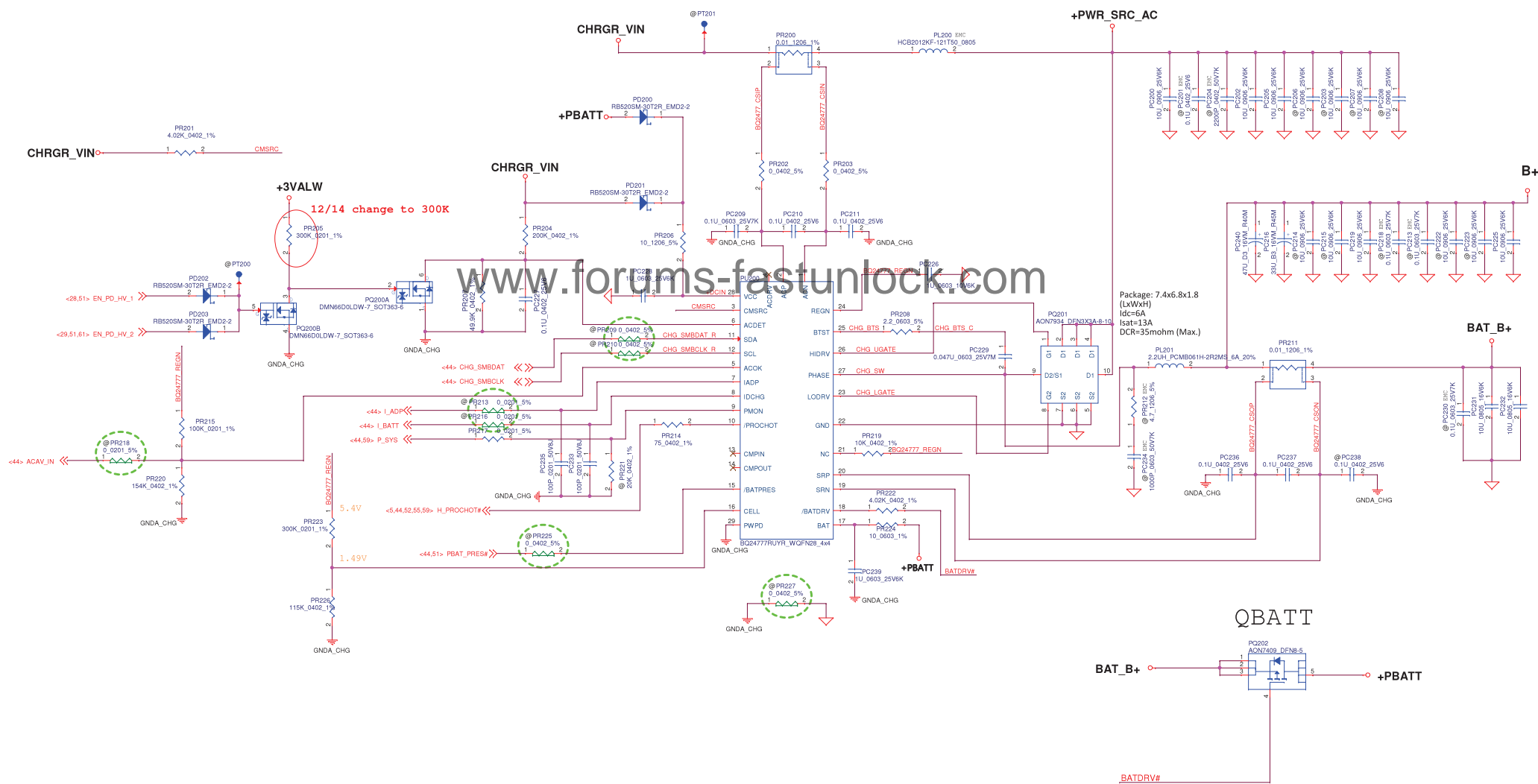
07/22 All to @



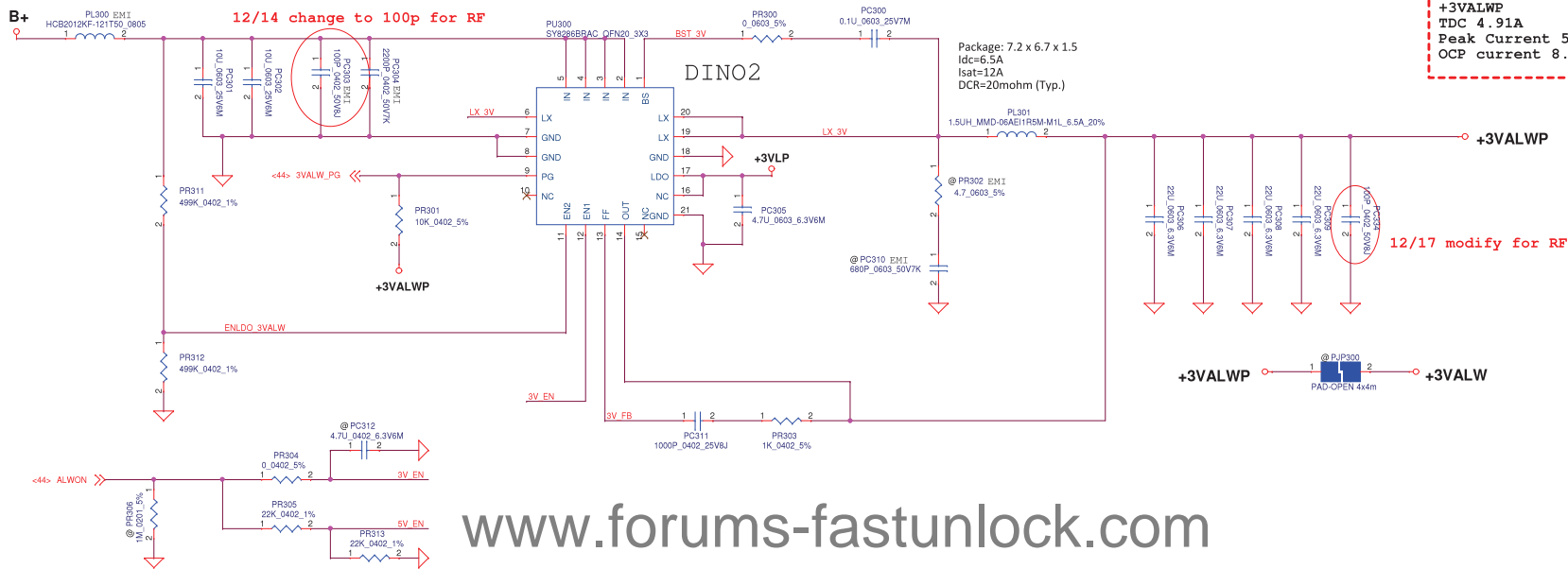
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								Size		Document Number		Rev	
								LA-D311P				0.1	
								Date:		Friday, December 25, 2015		Sheet 52 of 60	

Charger controller(40.1), Support component(40.2)

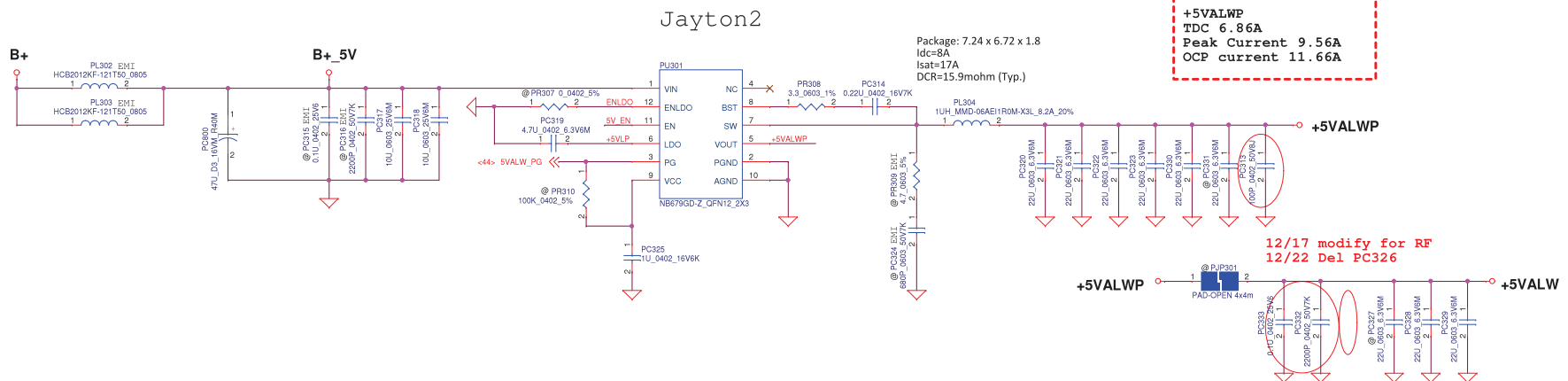


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date		2015/06/10	Deciphered Date		2015/06/10	Title
P53 - PWR Charger BQ24777						Rev 0.1
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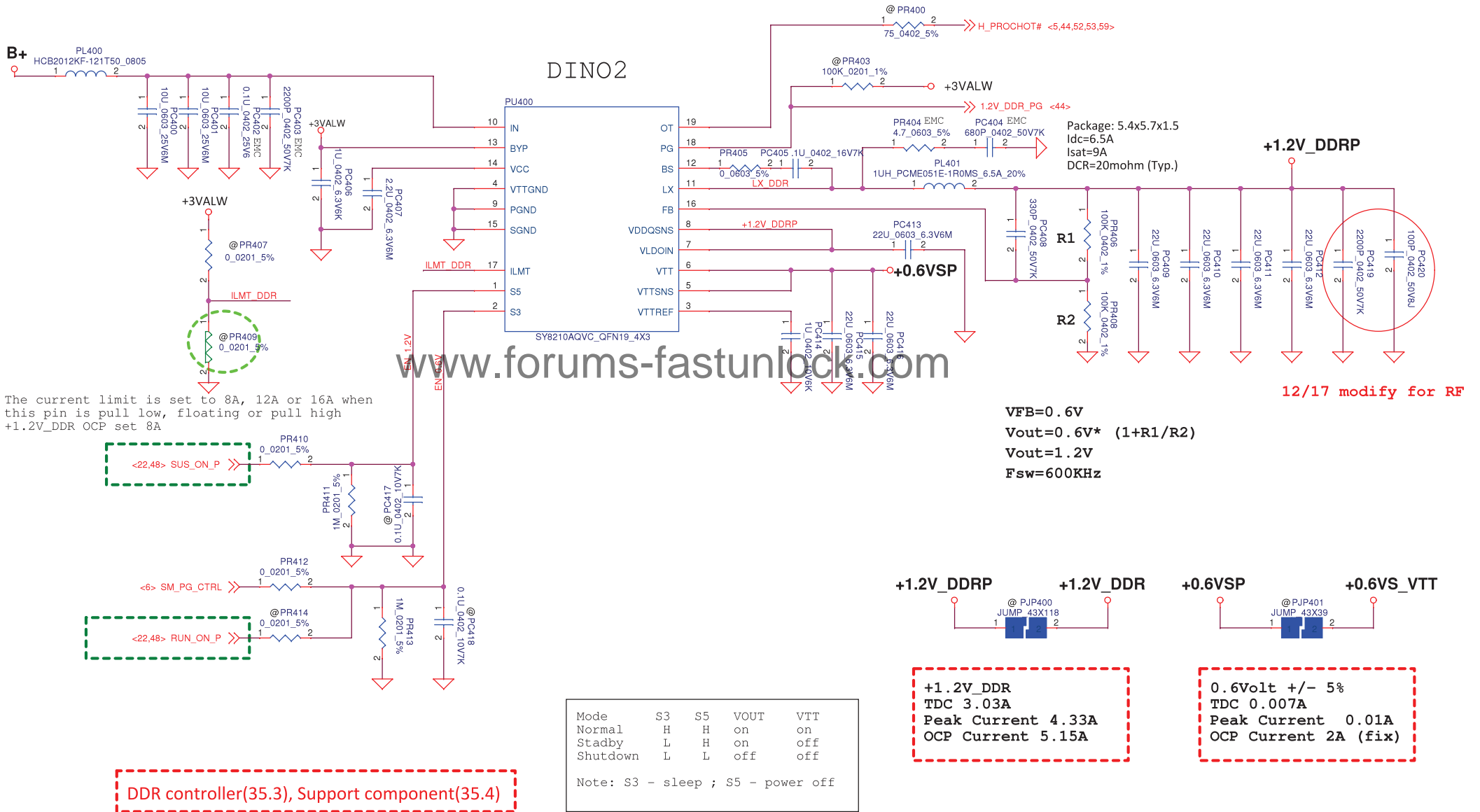


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3V/5V controller(35.1), Support component(35.2)



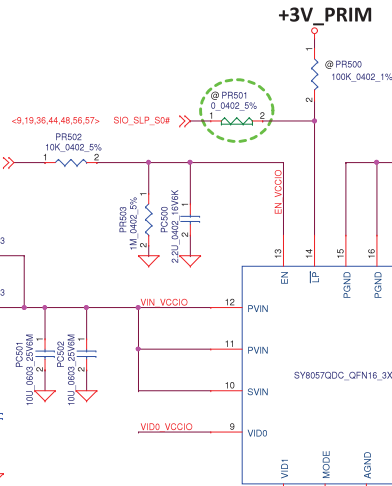
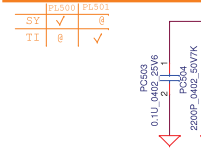
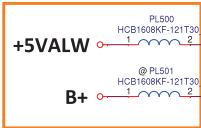
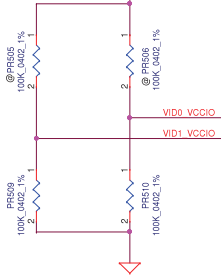
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Issued Date	2015/06/10	Deciphered Date	2015/06/10	Title	
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SY8057 Rmode = 200k				
TP	VID1	VID0	Vout(V)	
0	X	X	0.000	
1	0	0	0.850	
1	0	1	0.875	
1	1	0	0.950	
1	1	1	0.975	

+3V\_PRIM



JAYTON

VCCIO  
TDC 2.1A  
Peak Current 3 A  
OCP Current 4.2 A Fix by IC  
MIN:3.6A  
MAX:4.9A  
Choke DCR 43.0mohm

Vout=0.85V  
+0.85VS\_VCCIO

12/14 change to EMI part for RF

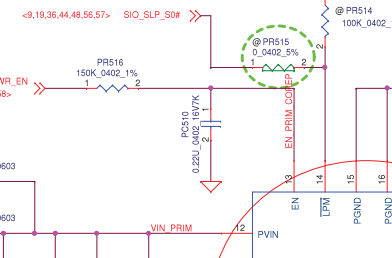
Fsw=1.2MHz

+0.85VS\_VCCIO

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+3VALW



12/21 SY change to TI

JAYTON

PRIM\_CORE  
TDC 0.77A  
Peak Current 1.1A  
OCP Current 4.2 A Fix by IC  
MIN:3.6A  
MAX:4.9A  
Choke DCR 43.0mohm

Vout=1V  
+0.95V\_PRIM

Fsw=1.2MHz

+0.95V\_PRIM

12/14 change to EMI part for RF

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

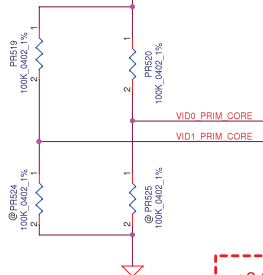
Fsw=1.2MHz

Fsw=1.2MHz

Fsw=1.2MHz

TPS62134D			
TP	VID1	VID0	Vout(V)
0	X	X	0.700
1	0	0	0.850
1	0	1	0.900
1	1	0	0.950
1	1	1	1.000

+3VALW

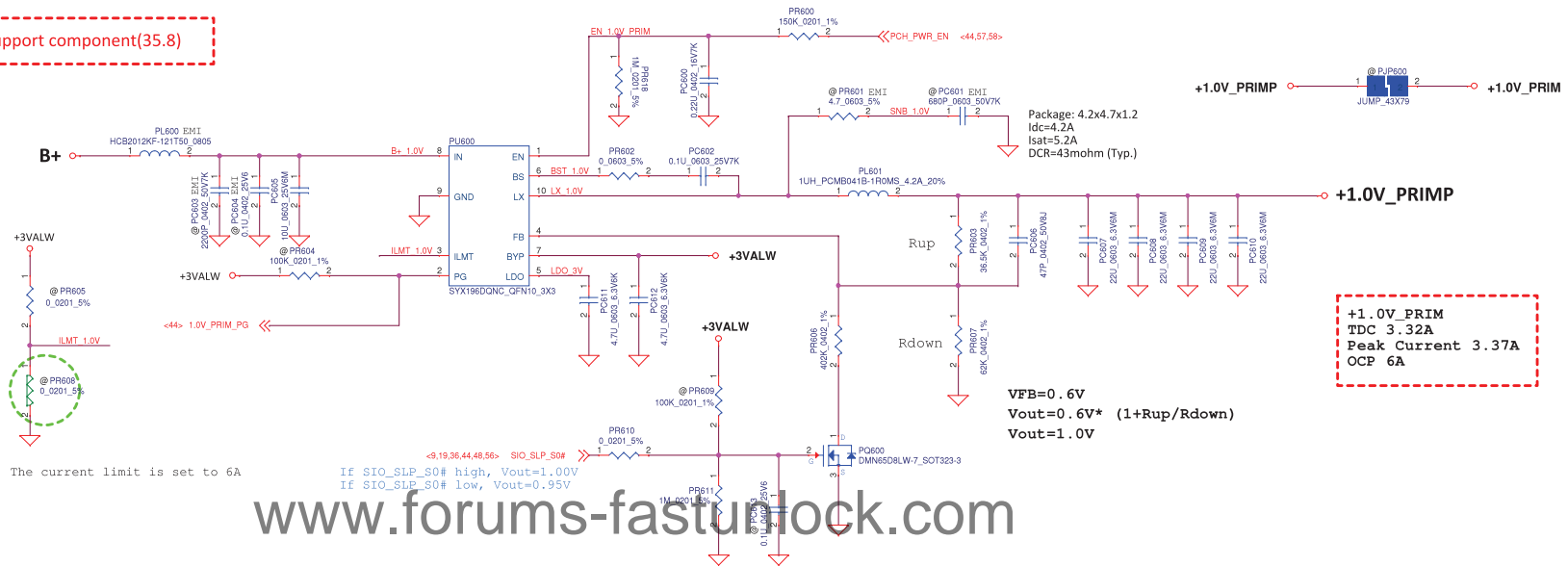


+0.85VS\_VCCIO controller(35.21), Support component(35.22)  
+0.95V\_PRIM controller(35.23), Support component(35.24)

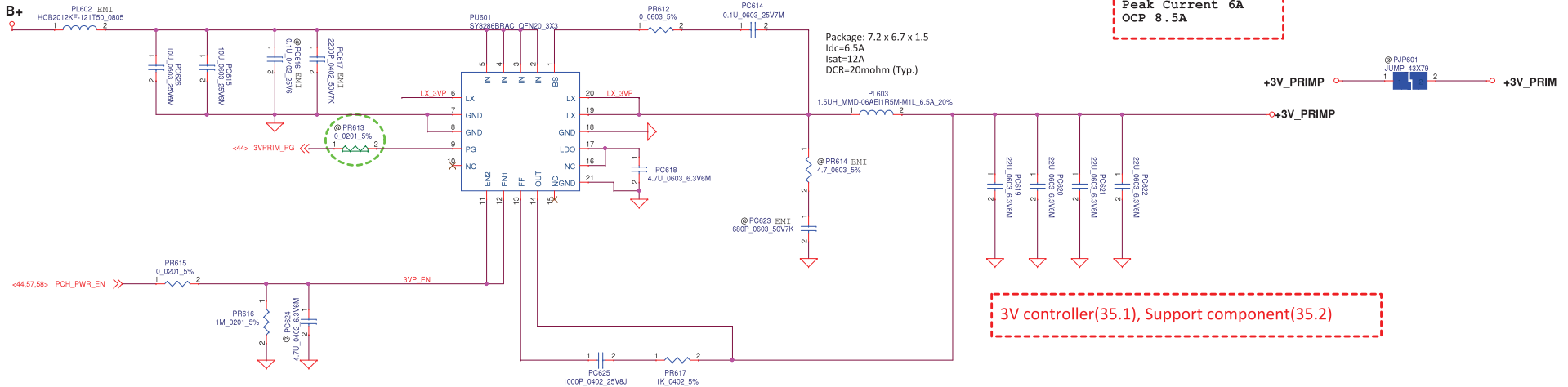
12/21 change for TI mode

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+1.0V\_PRIM controller(35.7), Support component(35.8)



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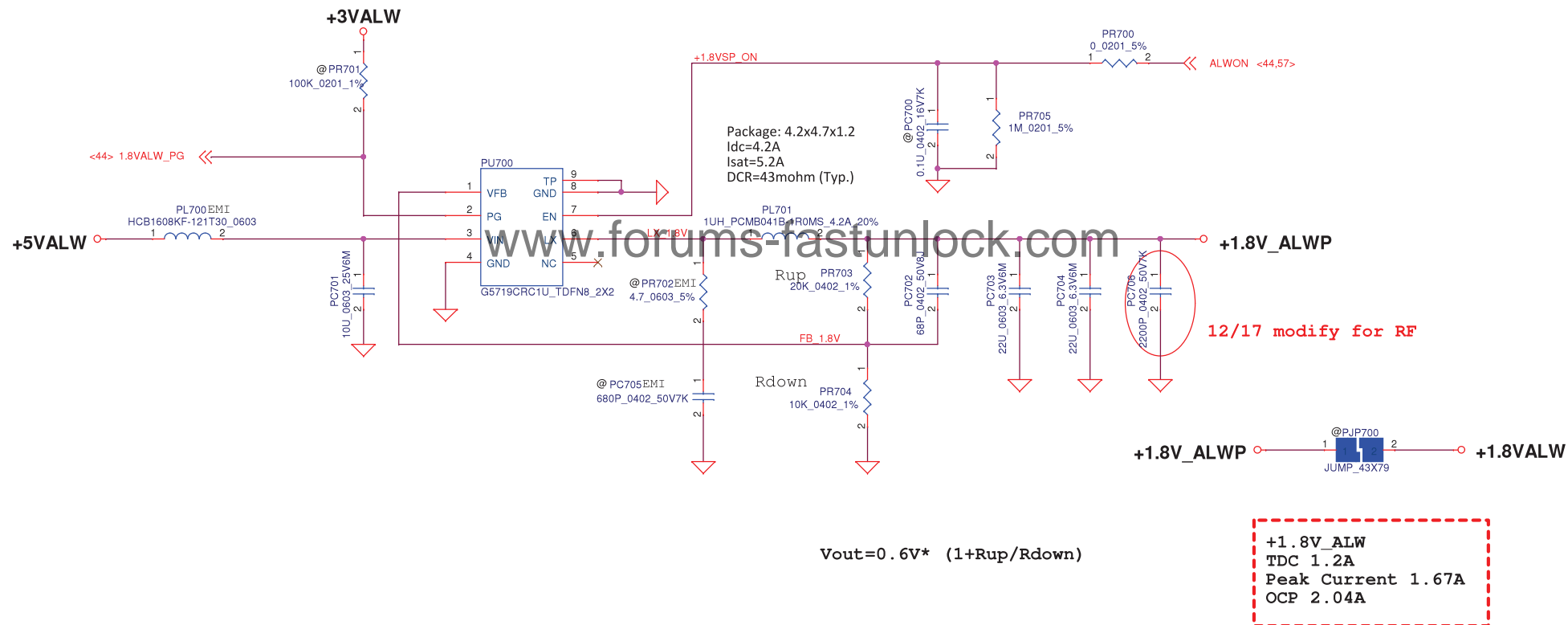


3V controller(35.1), Support component(35.2)

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		P57 - PWR +1.0V PRIM/+3V PRIM
		Size
		LA-D311P
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		0.1
		Date: Friday, December 25, 2015
		Sheet 57 of 60

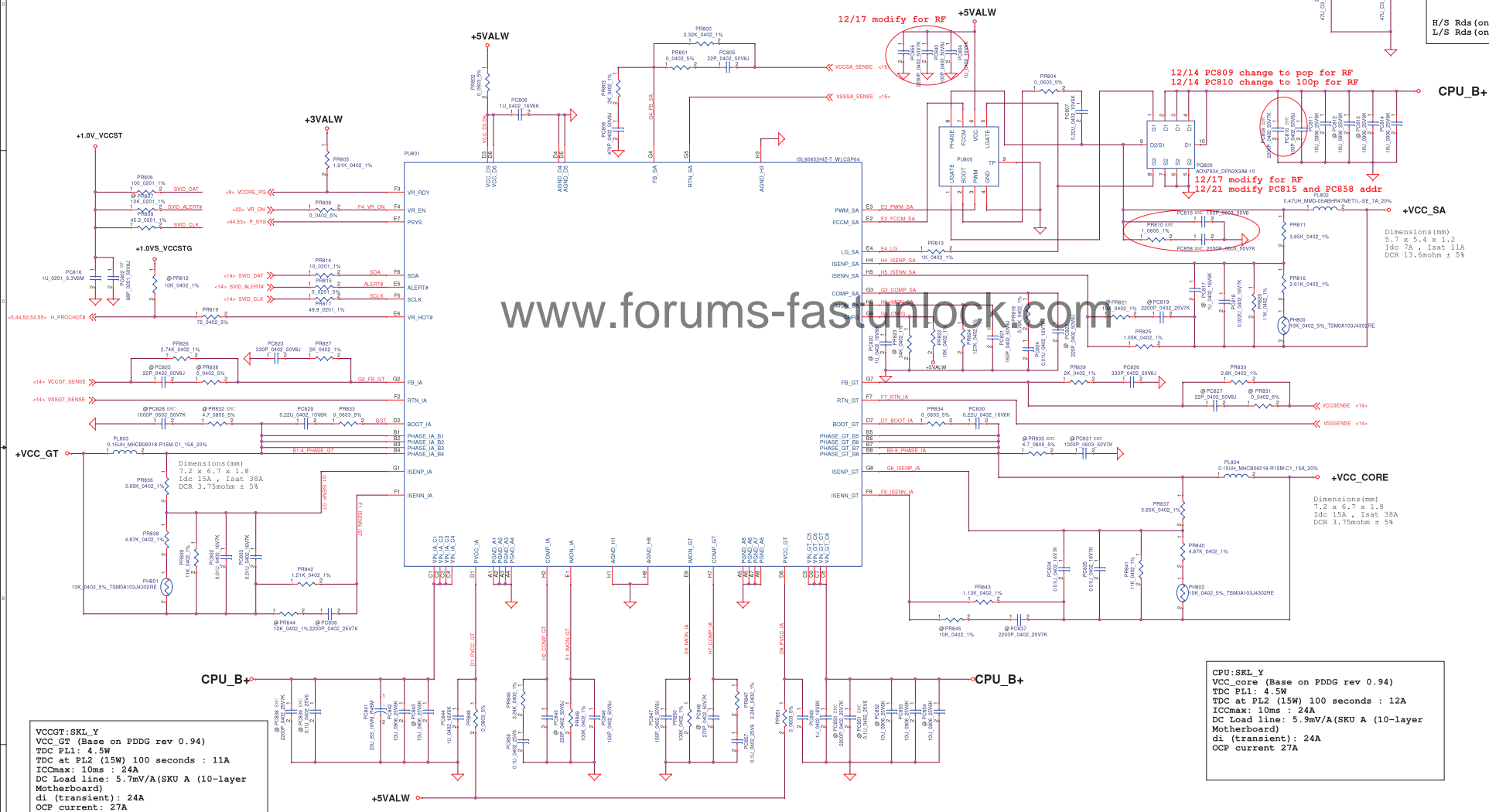


1.8V controller(35.15), Support component(35.16)



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VCORE/GT/SA controller(36.1), Drivers(36.2), Support component(36.3)



```
VCCSA:SKL_Y
VCC_SA (Base on PDDG rev 0.94)
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 4A
ICMax 10ms : 4A
DC Load line: 17.9mV/A (SKU A (10-layer
Motherboard)
di (transient): 4A
OCP current: 6.97A
```

	TYP	MAX
H/S Rds (on) 4.5V	:12.4 mohm	, 15.8 mohm
L/S Rds (on) 4.5V	:9.1 mohm	, 11.6 mohm

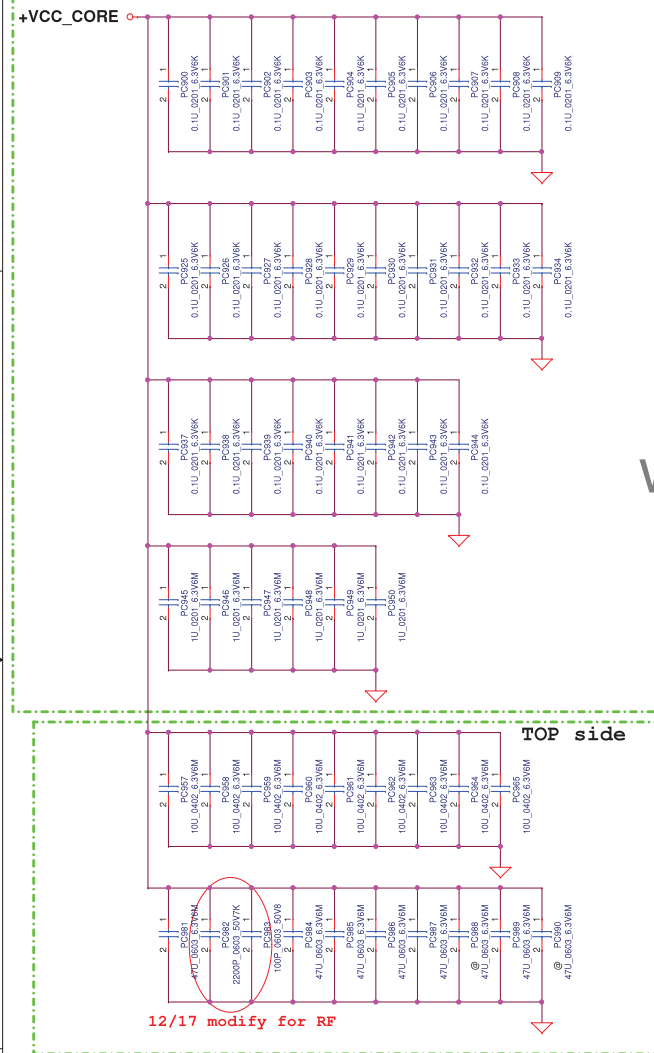
```
CPU:SKL_Y
VCC_core (Base on PDDG rev 0.94)
TDC PL1: 4.5W
TDC at PL2 (15W) 100 seconds : 12A
ICCMax: 10ms : 24A
DC Load line: 5.9mV/A(SKU A (10-layer
Motherboard)
di (transient): 24A
OCP current 27A
```

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				Date	1999-12-28 25:2015 19:56 59 of 80

VCC\_GT  
0.1U\_0201 \* 15 pcs +1U\_0201\*6 pcs+1U\_0402\*4pcs+10U\_0402\*2pcs+47U\_0603\*13pcs

VCC\_CORE  
0.1U\_0201 \* 28 pcs +1U\_0201\*6 pcs+10U\_0402\*9pcs+47U\_0603\*10pcs

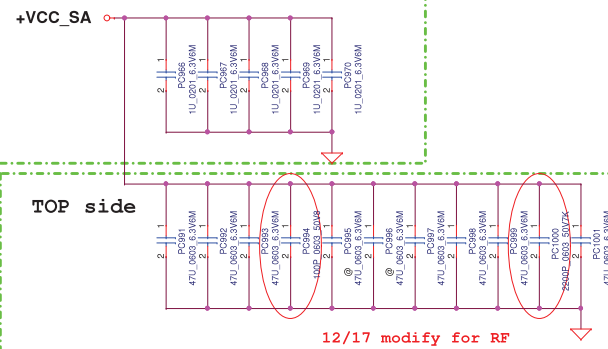
Back side



VCC\_CORE output cap (36.4)

VCC\_SA  
1U\_0201 \* 5 pcs +47U\_0603\*11 pcs

Back side

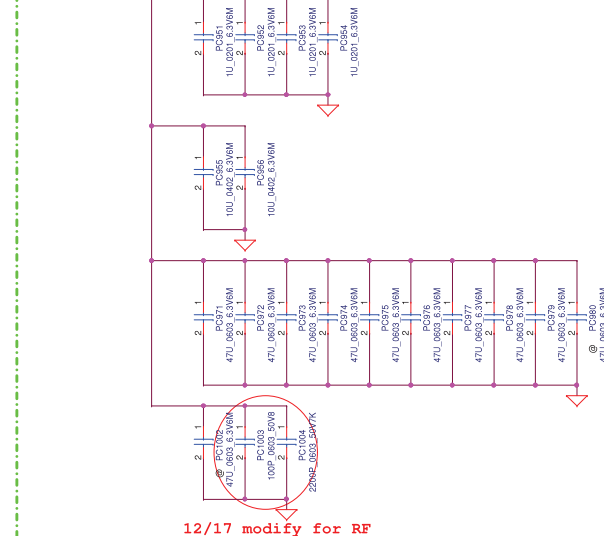


VCC\_SA output cap (36.6)

+VCC\_GT

Back side

TOP side



VCC\_GT output cap (36.5)

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					Document Number
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