

LCFC Confidential


GS454/GS554(NMD031) MB Schematics Document

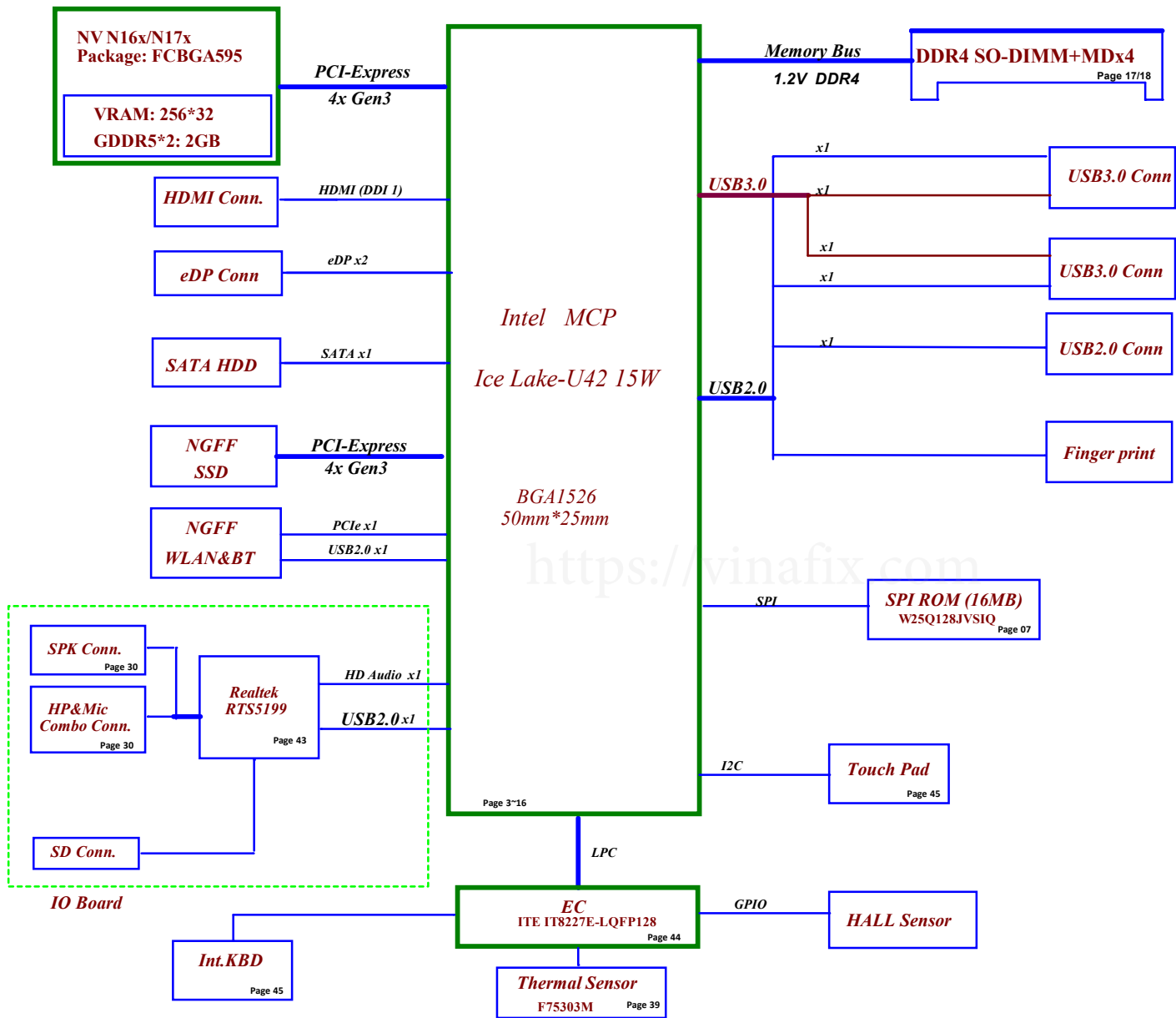
ICL U42 with DDR4 + Nvidia N16V-GM

2019-10

REV: 0.1

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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		Cover Page	
2015/08/20		2016/08/20			
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Size	Document Number			Rev	
C	GS44D/GS54D			0.1	
Date:		Friday, December 06, 2019		Sheet	1 of 60



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WIMAX
EC_SMB_CK1 EC_SMB_DAI	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DAI	IT8227E +3VS	X	X	V +3VG_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DAI	IT8227E +3VAVL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	X

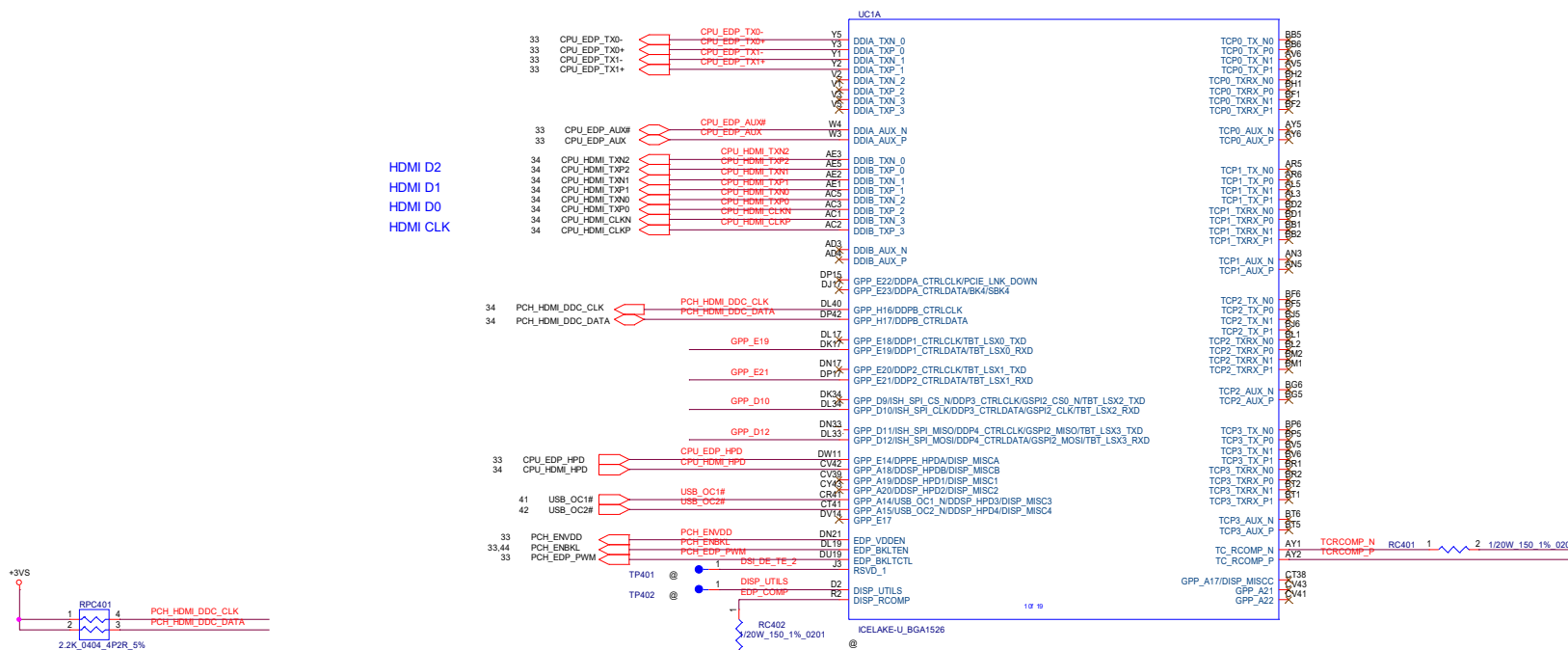
EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update				

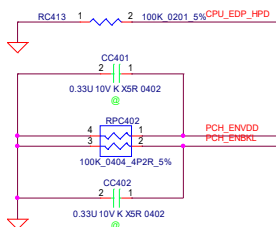
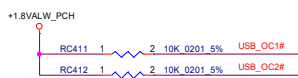
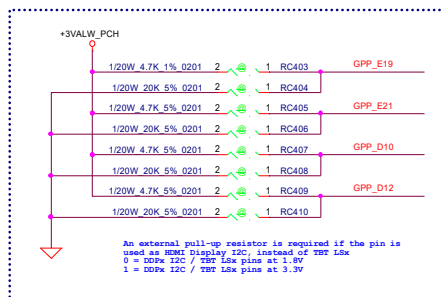
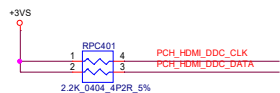
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5
	6
USB2.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5 Camera
	6 Touch Screen
	7 Finger Print
	8 Card Reader
	9 USB2.0 conn
	10 Bluetooth
PCIE	5~8 X4 DGPU
	9 WLAN
	10 NC
	11 SATA HDD
	12 NC
	13~16 X4 PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For Touch Pad Part



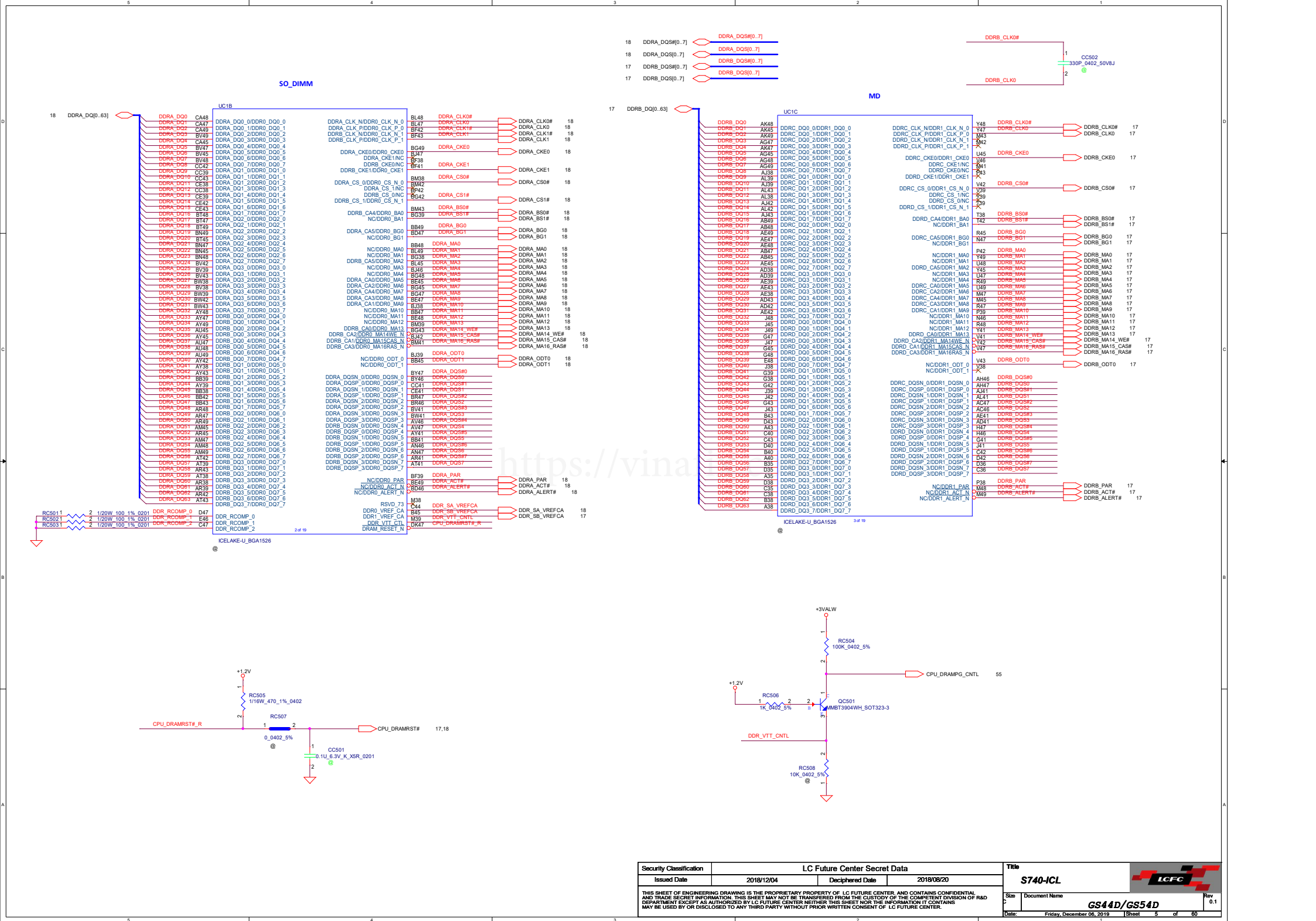
HDMI D2
HDMI D1
HDMI D0
HDMI CLK

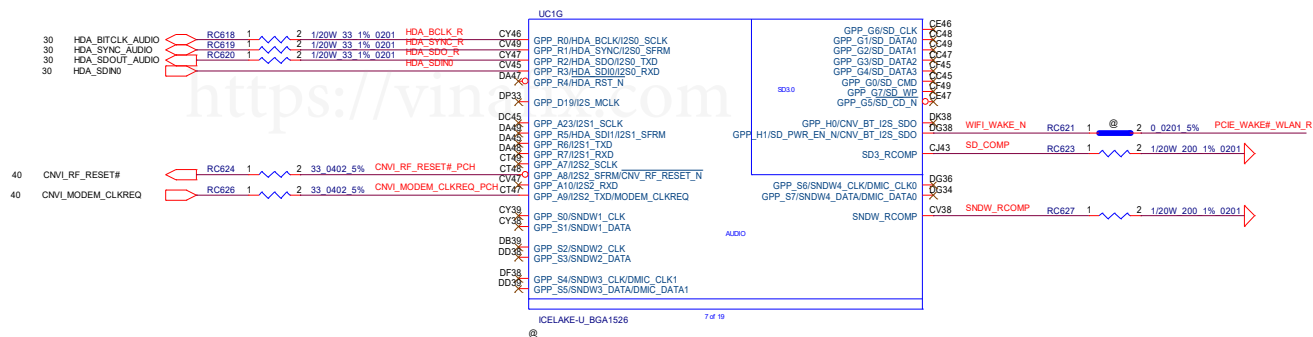
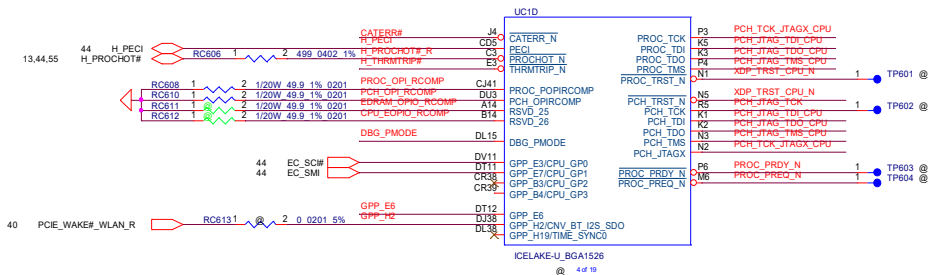
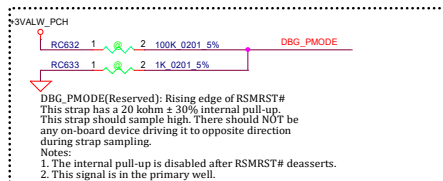
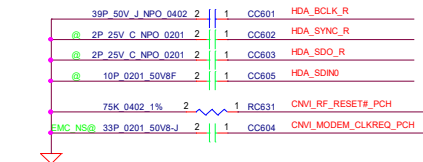
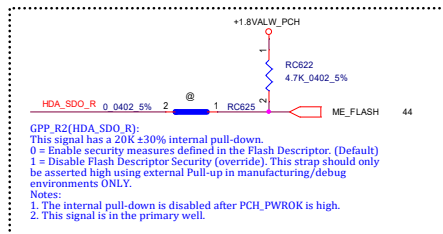
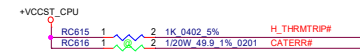
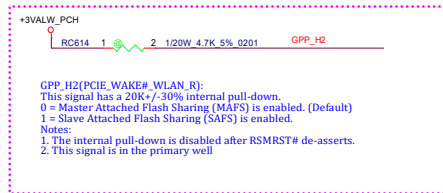
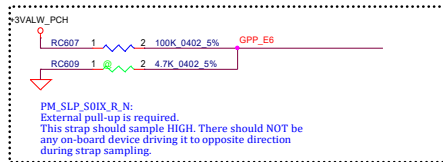
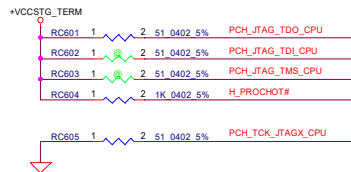


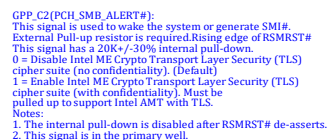
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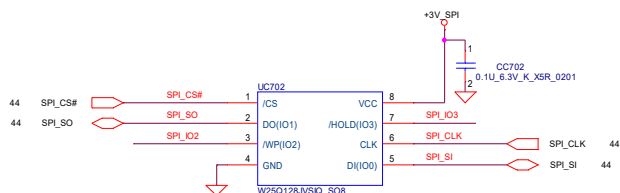
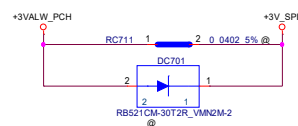
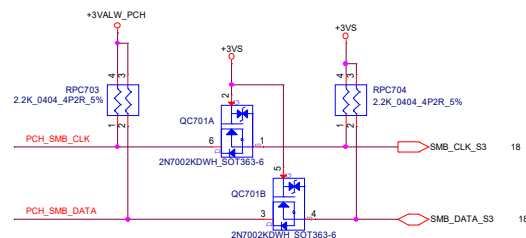
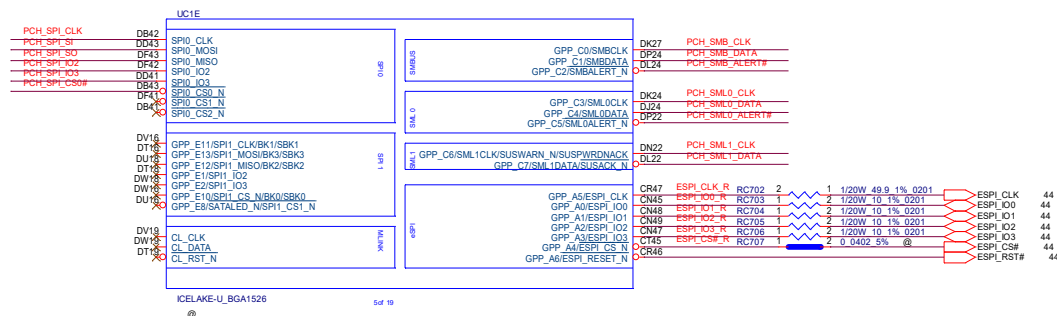
GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)

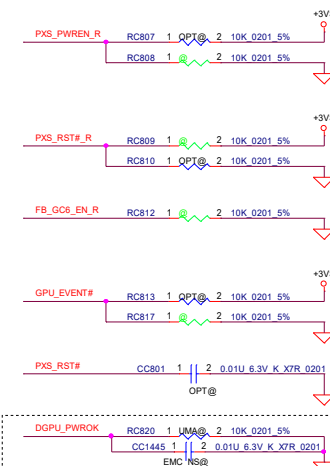
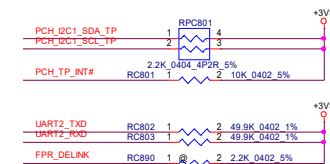
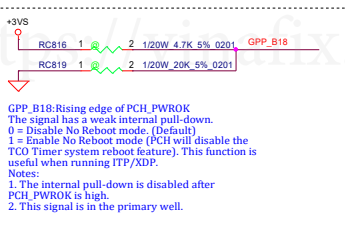
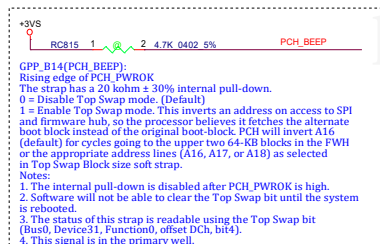
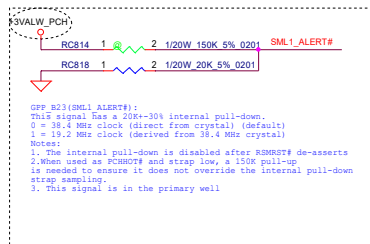
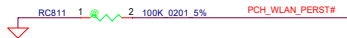
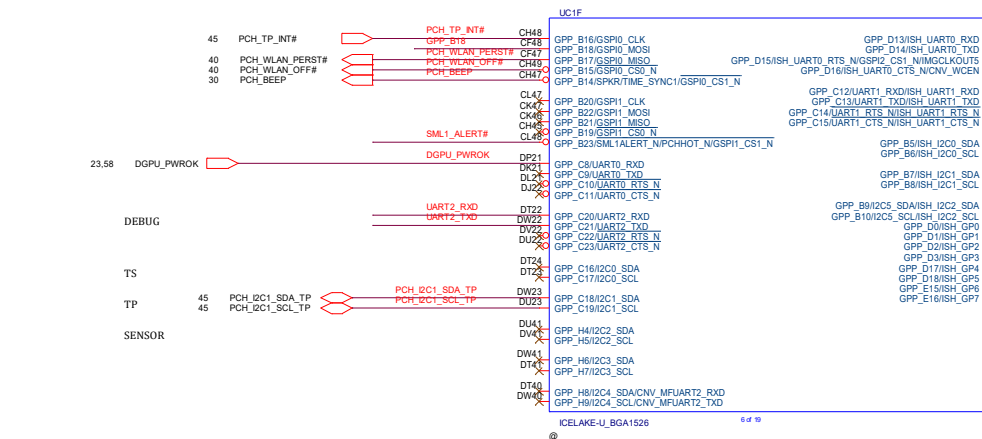


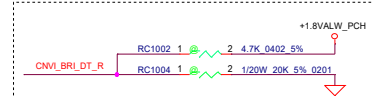
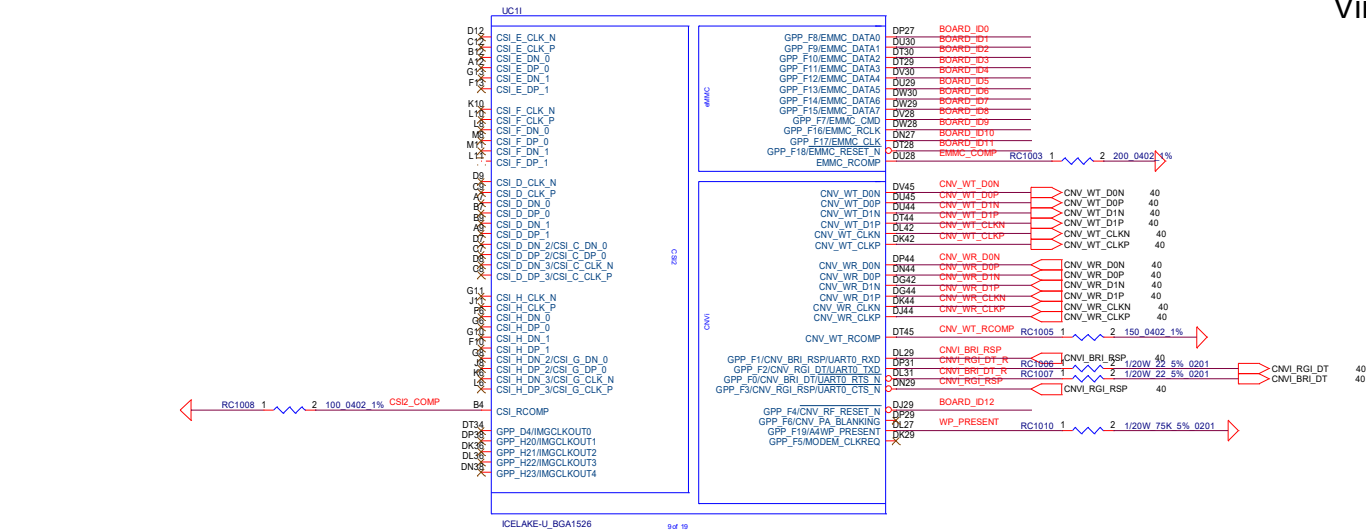




The diagram illustrates the timing relationship between the +3VSW_PCH input signal and several SPI-related signals and RC components. The signals shown are PCH_SPL_CS0#, PCH_SPL_SI, PCH_SPL_IO2, and PCH_SPL_IO3. The RC components are labeled RC715 through RC721. The timing parameters indicate specific delays and setup times, such as 150K, 0402, 5%, 2, 1, 2, 49.9, 0402, 1%, 1, 2.



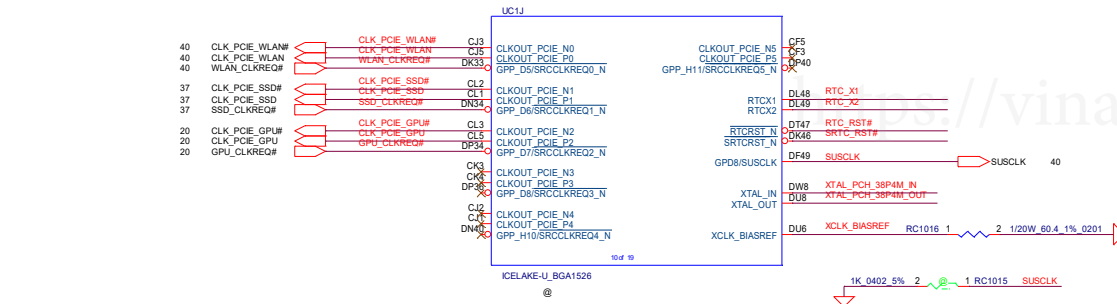
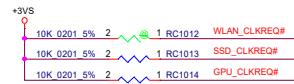


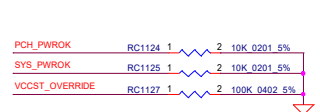
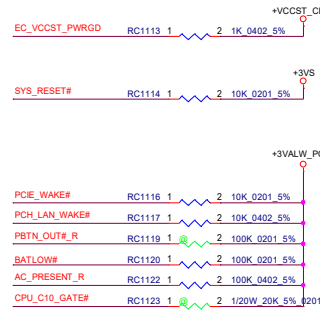
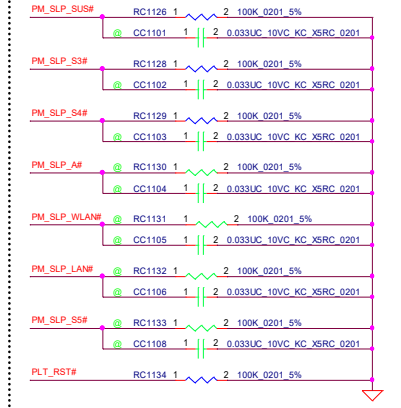
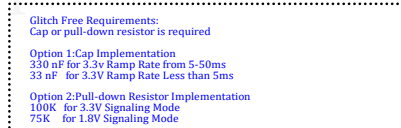
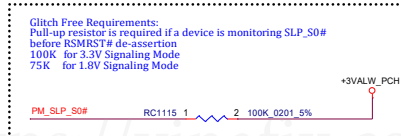
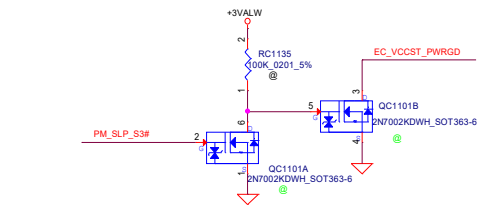
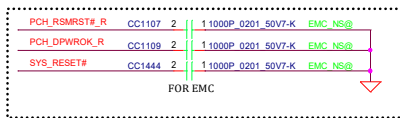
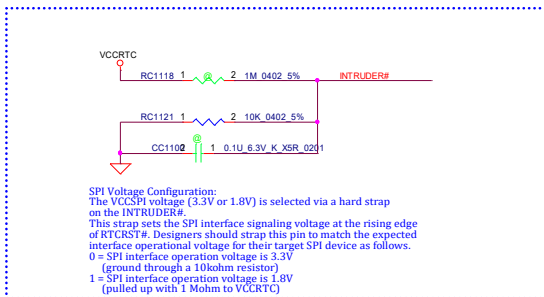
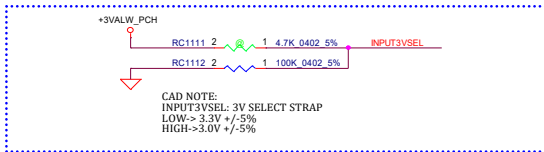
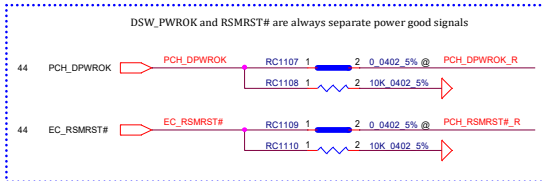
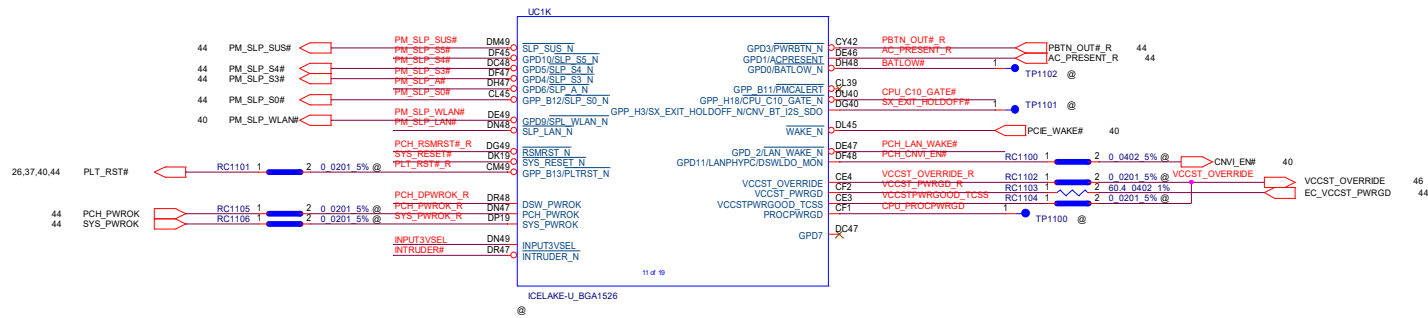


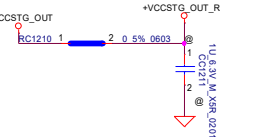
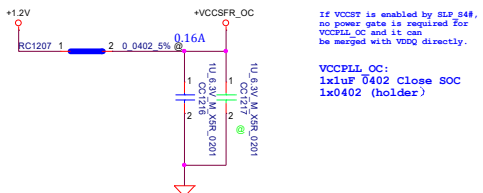
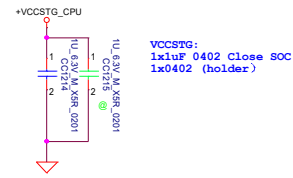
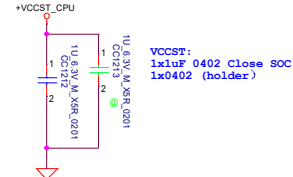
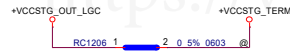
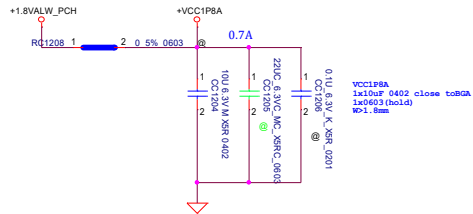
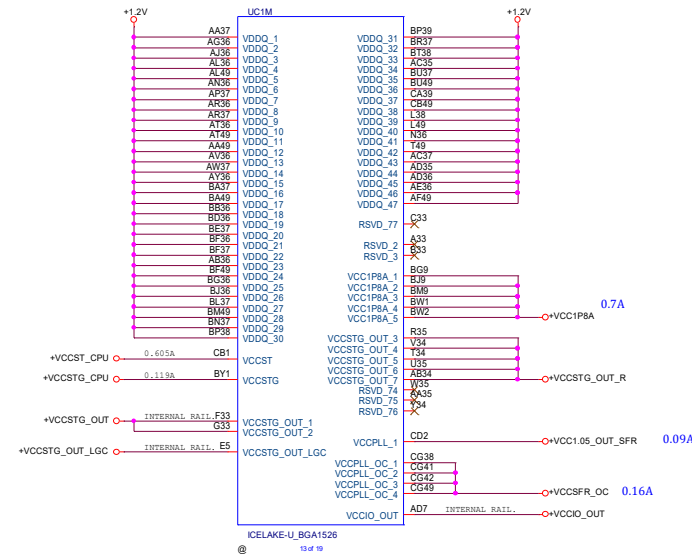
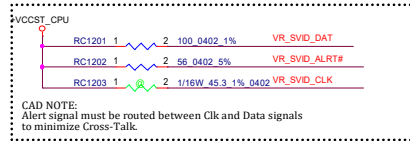
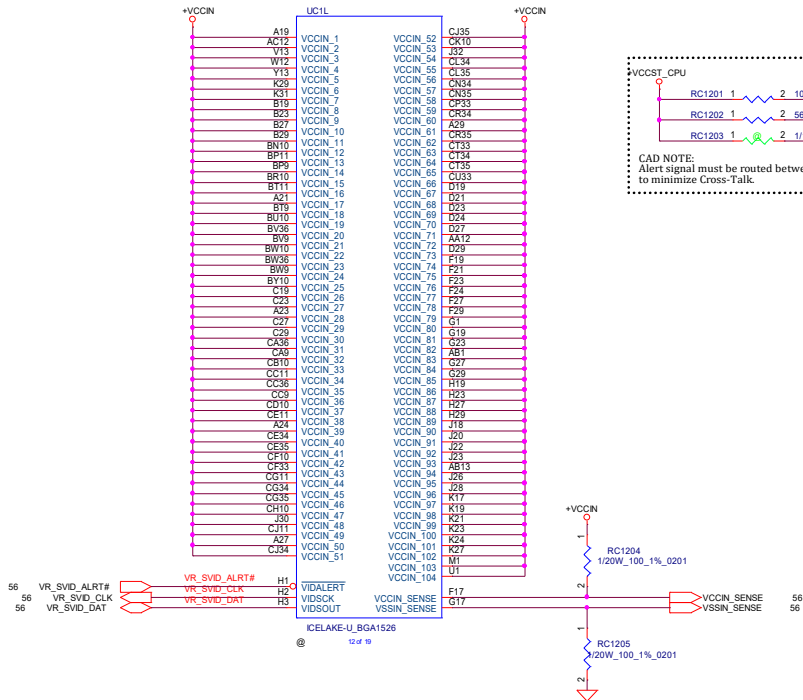
GPP_F0 /CNV_BRI_DT /UART0_RTS#
 XTAL Frequency Selection. Rising edge of RSMRST#
 This strap has a 20 kohm \pm 30% internal pull-down.
 This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.
 0 = 38.4 MHz (default)
 1 = 24 MHz
 Notes:
 1. The internal pull-down is disabled after RSMRST# de-asserts.
 2. This signal is in the primary well.

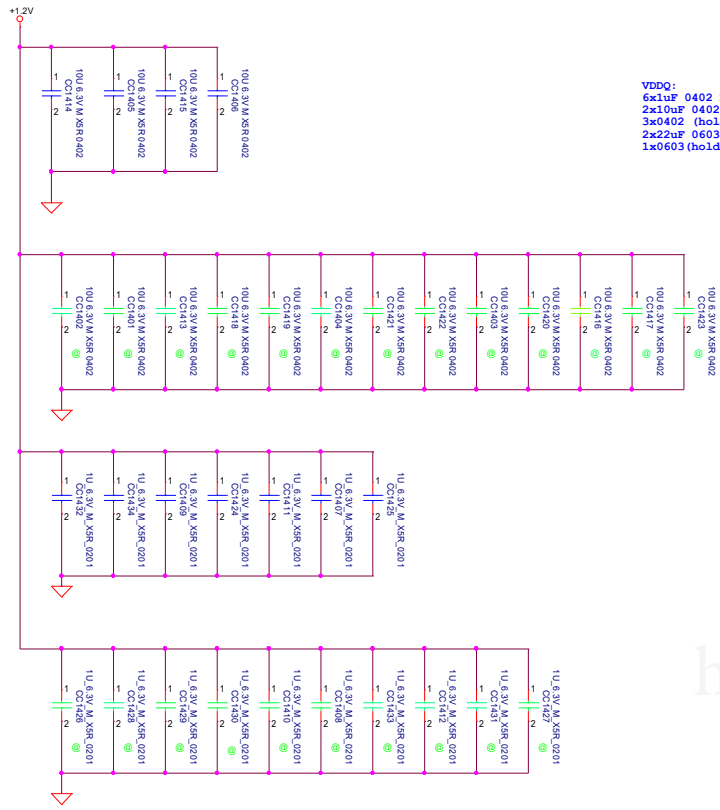


GPP_F2 /CNV_RGI_DT /UART0_TXD#
 M.2 CNV1 MODES. Rising edge of RSMRST#
 A weak external pull-up is required.
 0 = Integrated CNV1 enabled.
 1 = Integrated CNV1 disabled.
 Note:
 When a RF companion chip is connected to the PCH CNV1 interface, the device internal pulldown resistor will pull the strap low to enable CNV1 interface.



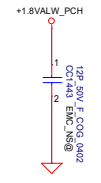
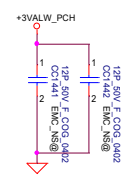
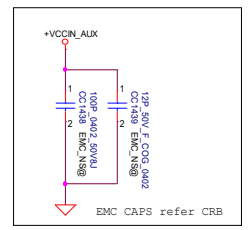
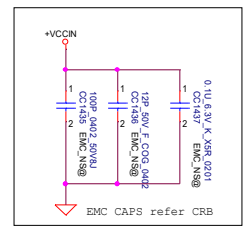


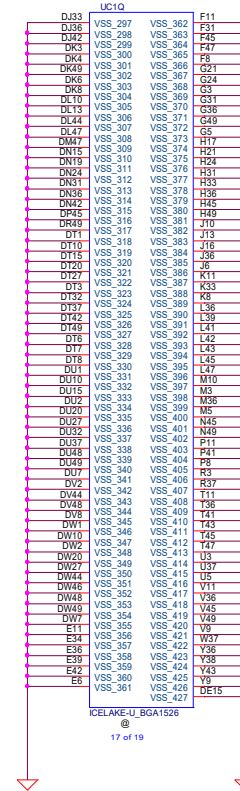
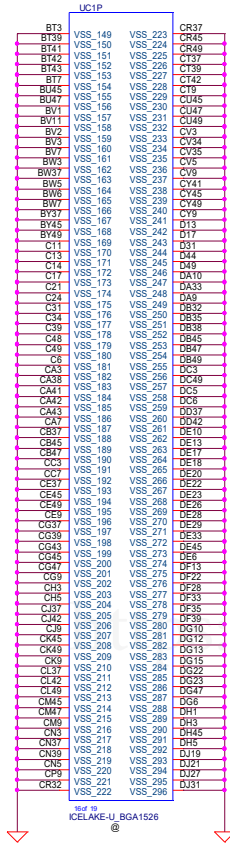
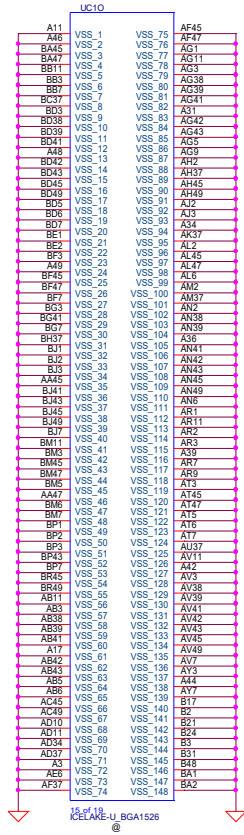




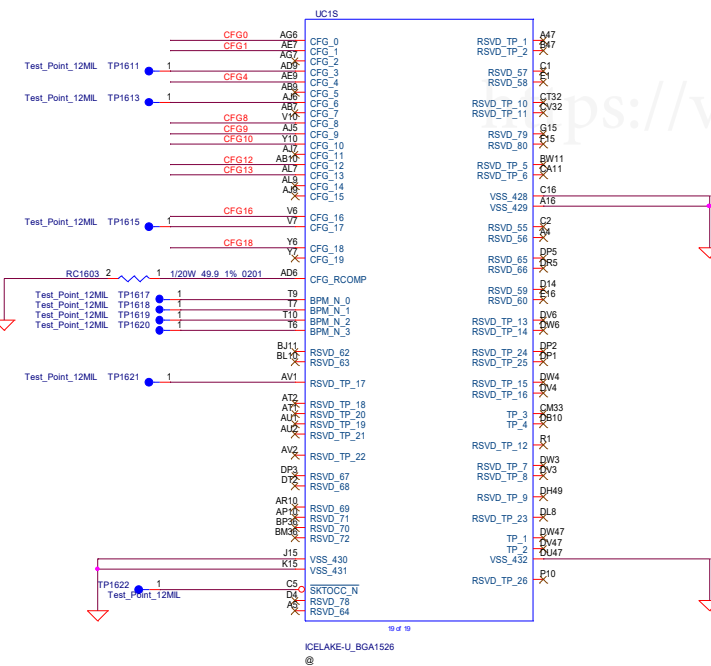
VDDQ:
6x10uF 0402 Back ,Outer row
2x10uF 0402 back Outer row
3x0402 (holder) back Outer row
2x22uF 0603 (SODIMM need)
1x0603 (holder)

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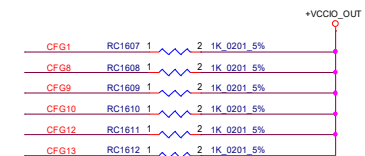




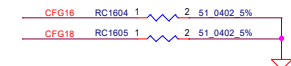
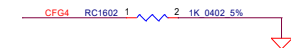
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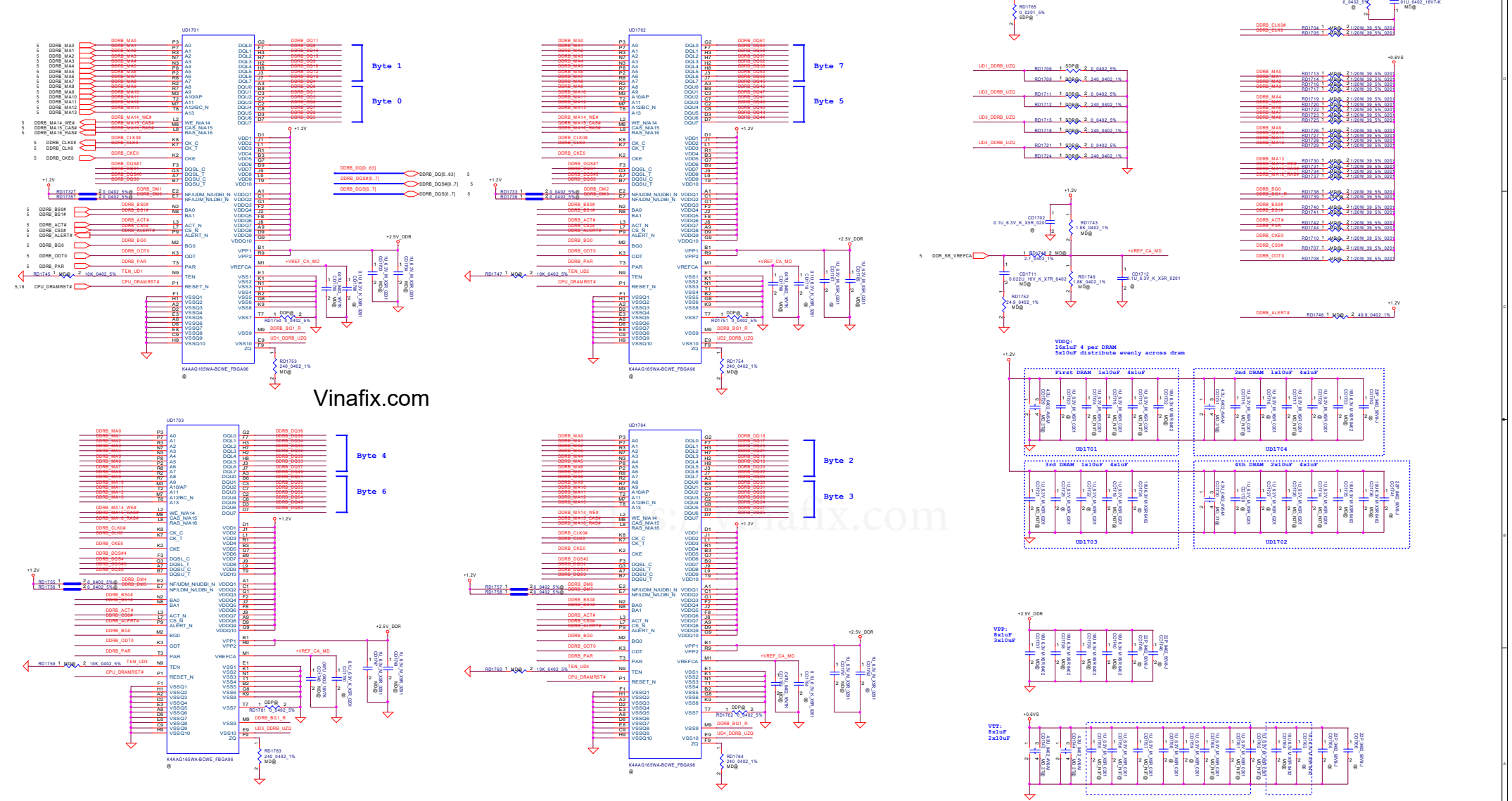
CFG0	1:Normal (Default) *
	0:Stall



CFG4	1:Disable
	0:Enable(Default)

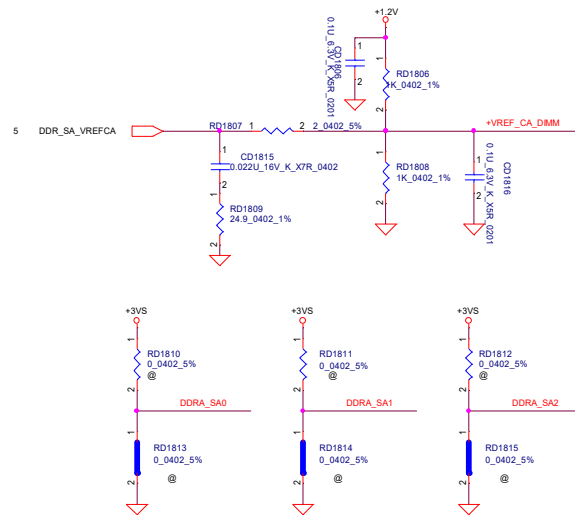
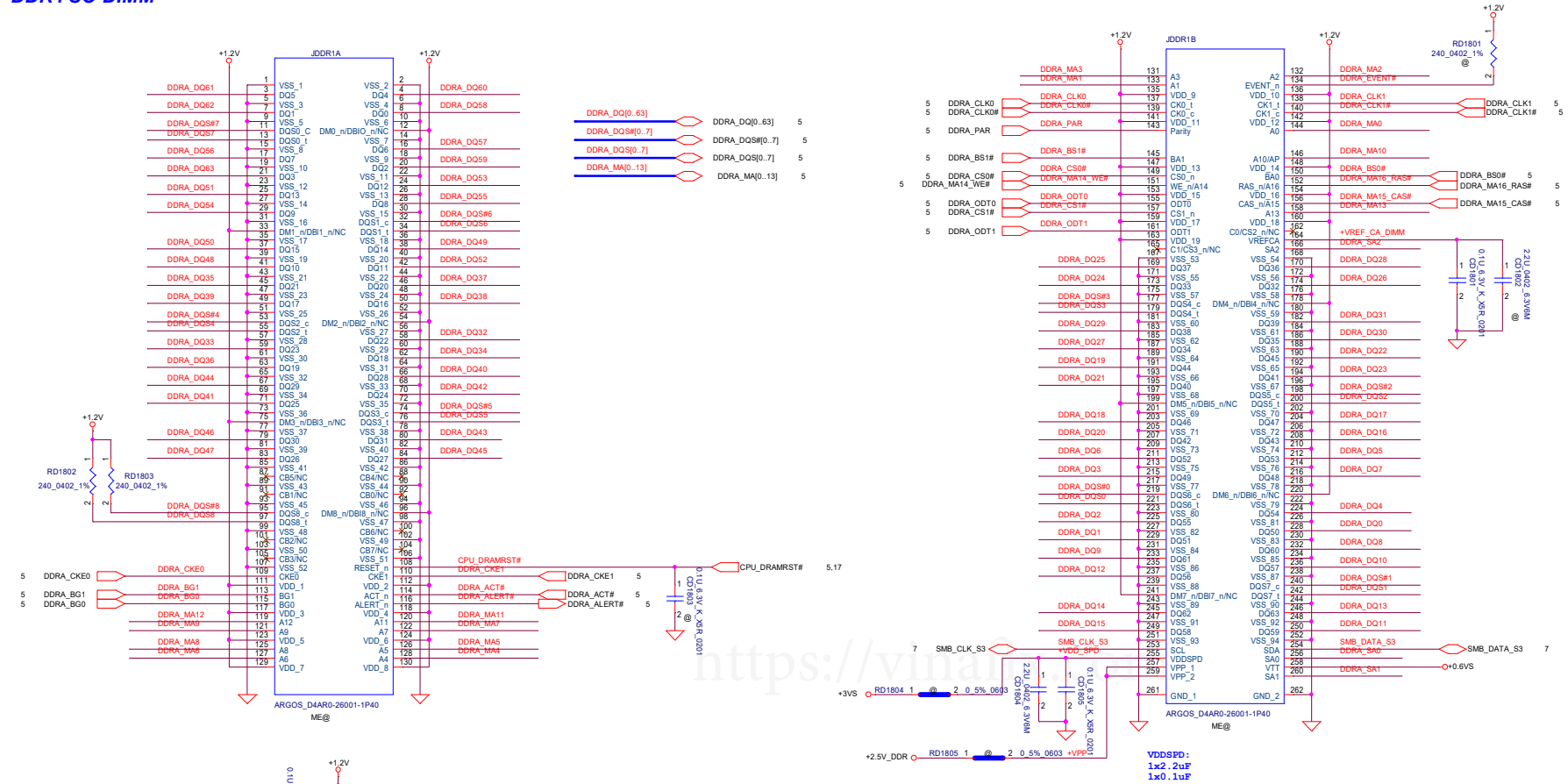


DDR4 Memory Down

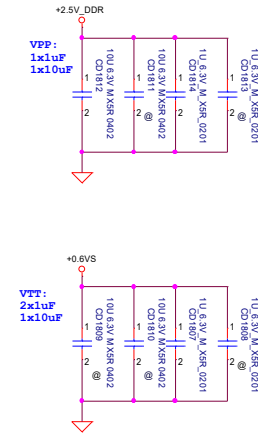
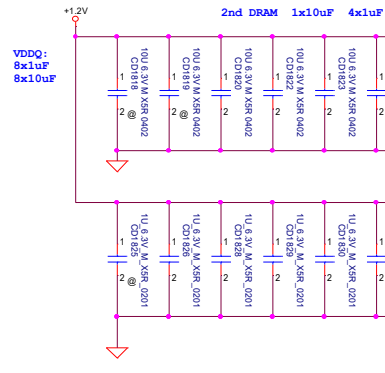



Security Classification				LC Future Center Secret Data				Title	
Issued Date		2017/06/24		Deciphered Date		2018/06/23		DDR4 Memory Down	
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DDR4 SO-DIMM



SPD Address = A0



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N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

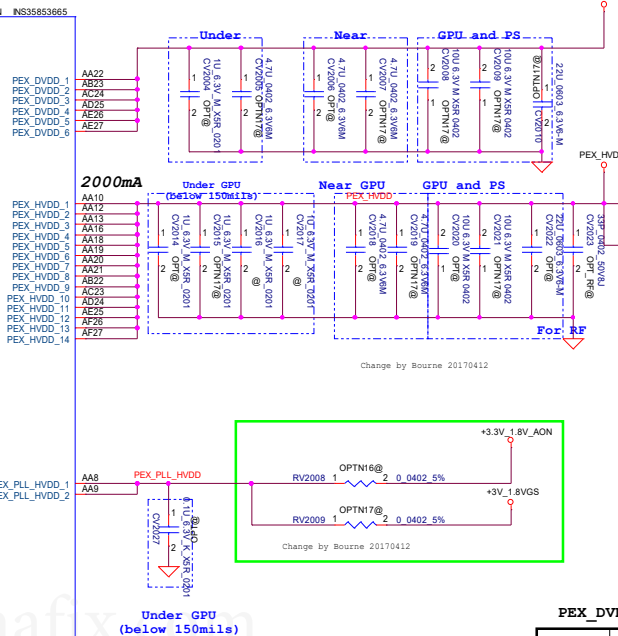
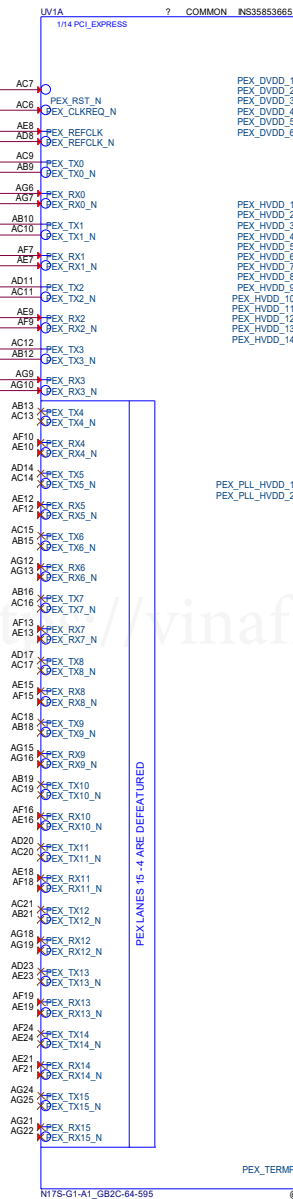
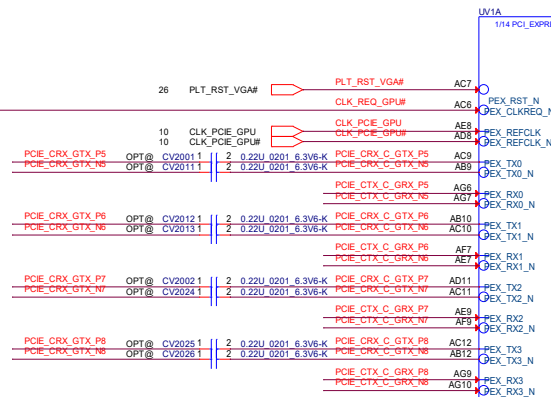
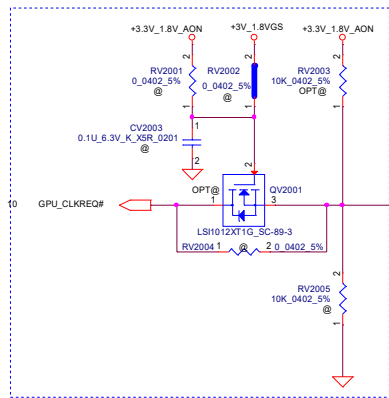
	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

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N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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PEX_DVDD
N16:+1.05VGS (recommend)
+1.0VGS (Used)
N17:+1.0VGS

PEX_HVDD
N16:+1.05VGS (recommend)
+1.0VGS (Used)
N17:+1.8VGS

PEX_PLL HVDD
N16:+3.3V AON
N17:+1.8VGS

PEX_DVDD/Q Decoupling





MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	
10uF	0	2	Midway
22uF	0	1	

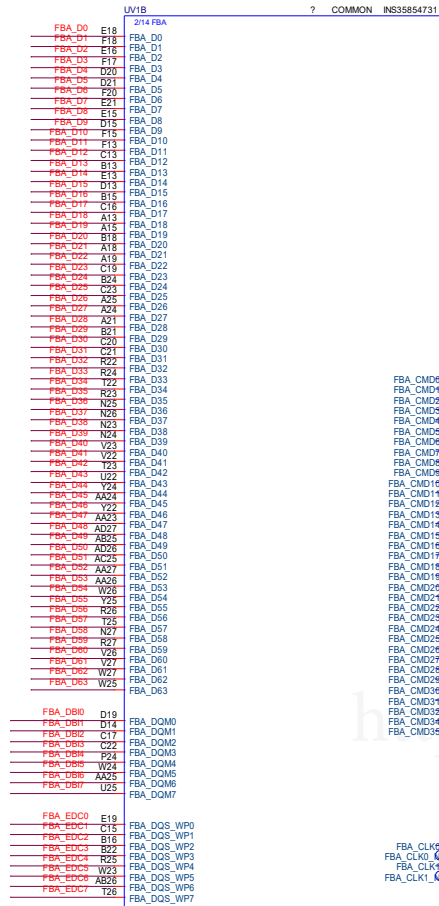
PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

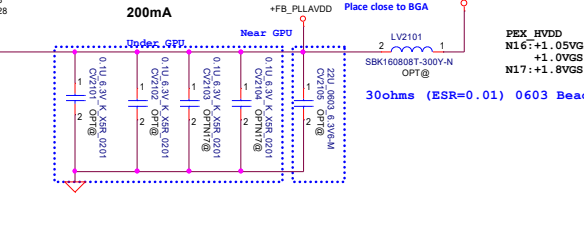
PEX_PLL HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

27.28 FBA_D0[0..63] 
27.28 FBA_CMD[31..0] 
27.28 FBA_EDC[7..0] 
27.28 FBA_DBI[7..0] 

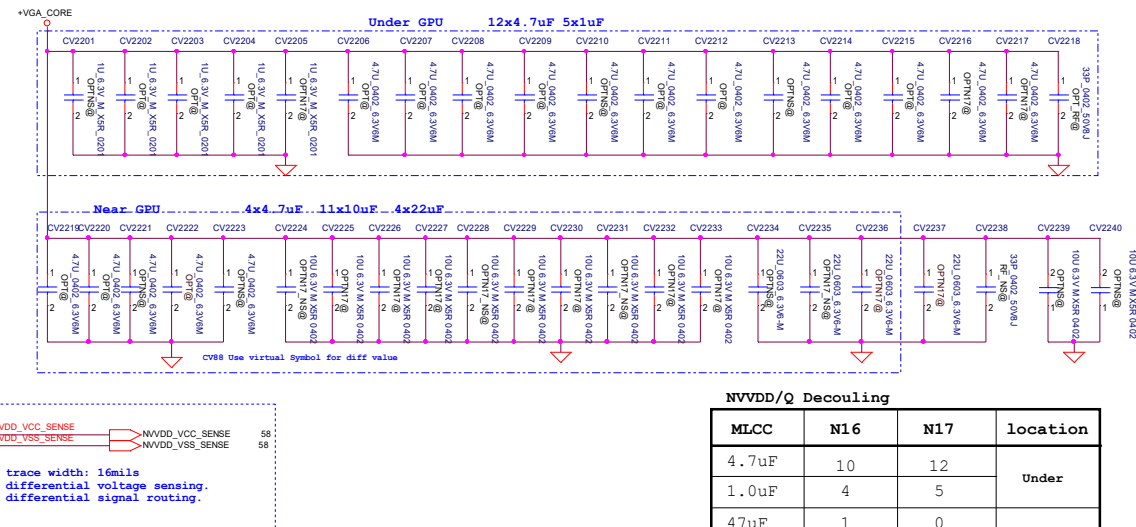
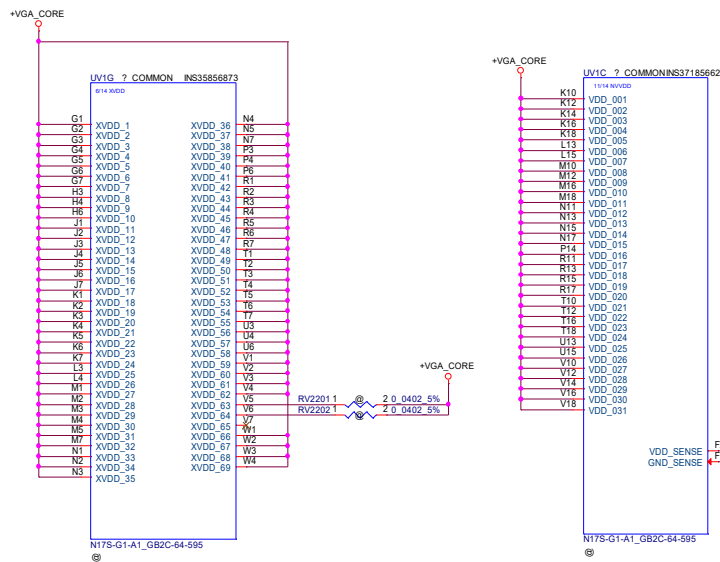


RV2101 10K 0402 1% OPT@
RV2102 10K 0402 1% OPT@
RV2103 10K 0402 1% OPT@
RV2104 10K 0402 1% OPT@
RV2105 2 60.4 0402 1%
RV2106 2 60.4 0402 1%



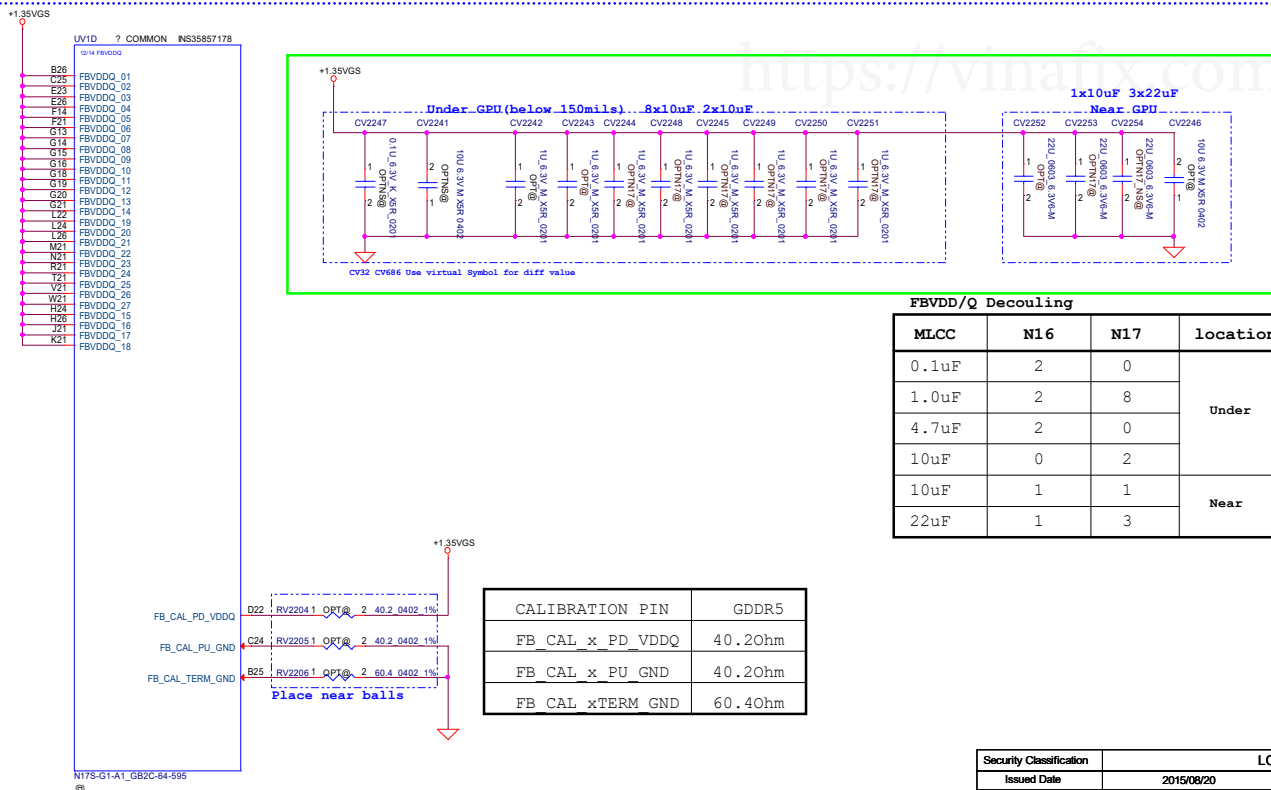
FB_PLL/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near



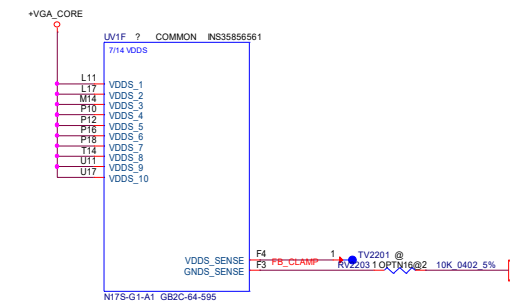
NVVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	



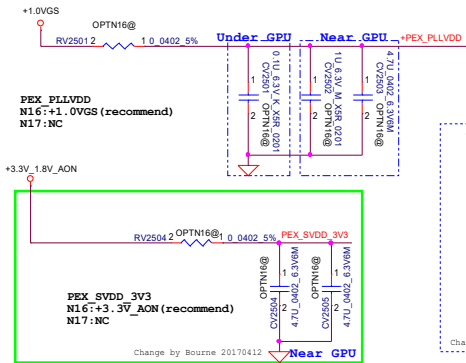
FBVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	Near
10uF	0	2	
10uF	1	1	
22uF	1	3	



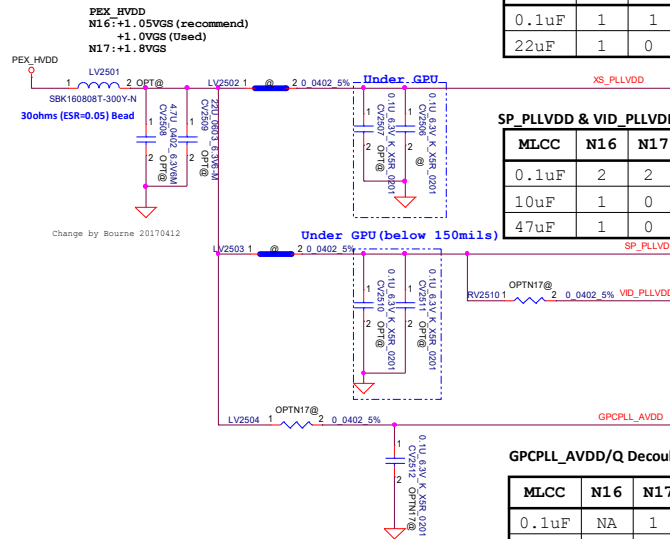
PEX_PLLVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	



PEX_SVDD/Q Decoupling

MLCC	N16	N17	location
4.7uF	2	NA	Near



XS_PLLVDD/Q Decoupling

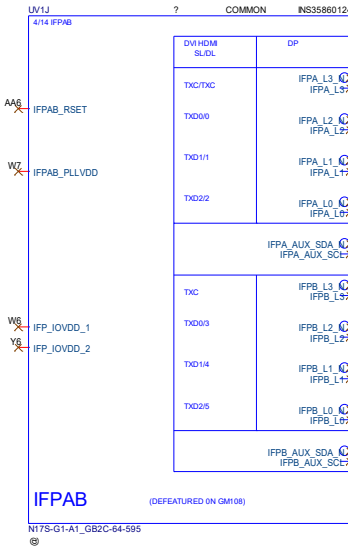
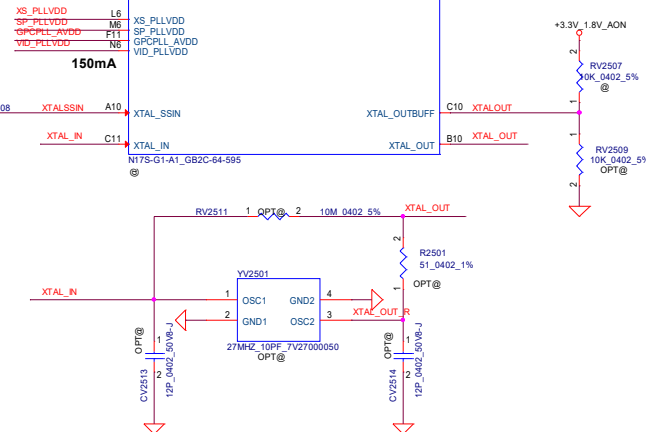
MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

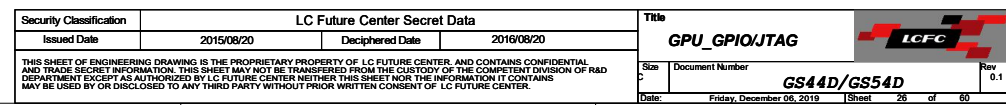
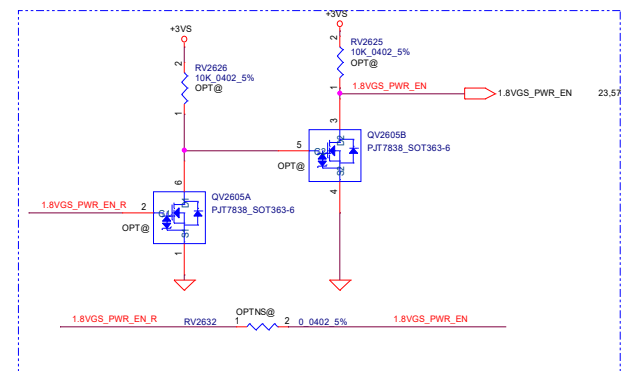
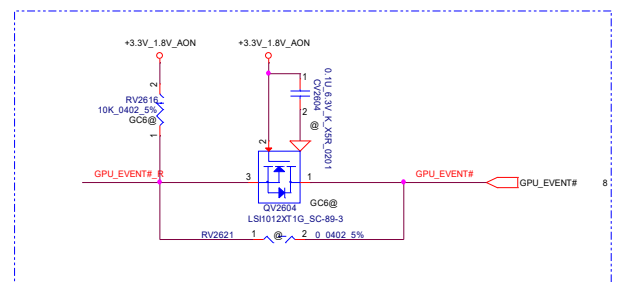
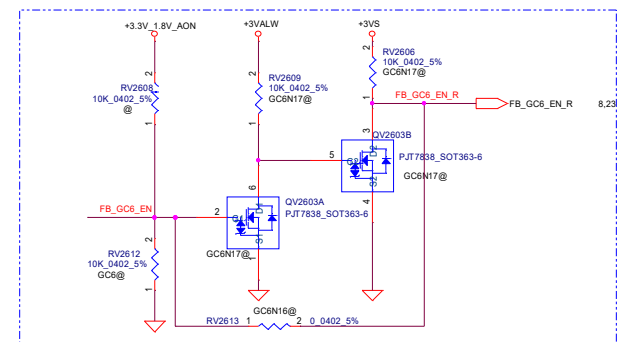
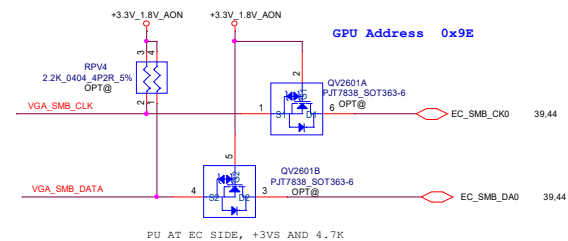
SP_PLLVDD & VID_PLLVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

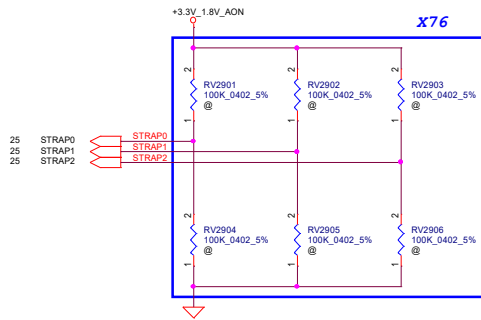
GPCPLL_AVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	

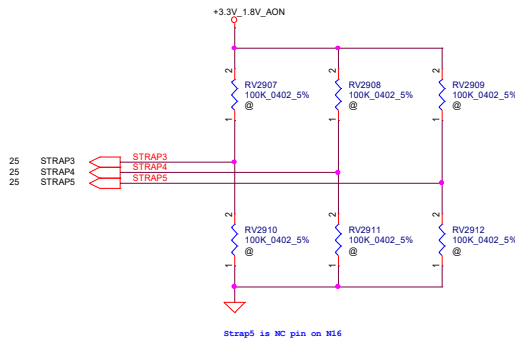




0.1



GPU	FB Memory (GDDR5)	RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0 (0x0000)	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1 (0x0001)	L	L
	Hynix 8Gb	H5GC8H24MJR-R0C	2 (0x0010)	L	H



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

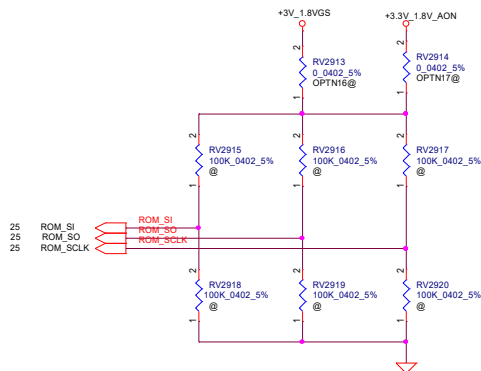
1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

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	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

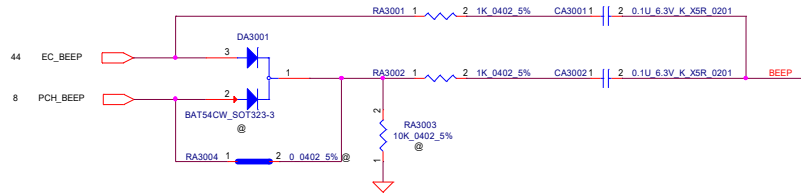
1: ENABLE 0: DISABLE
SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

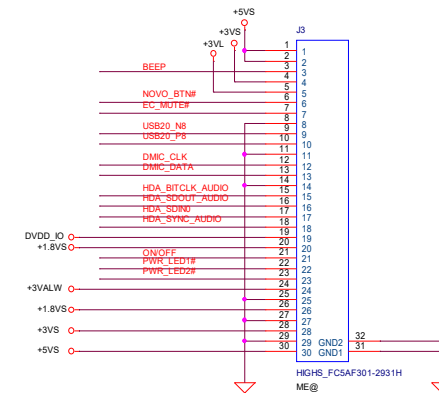
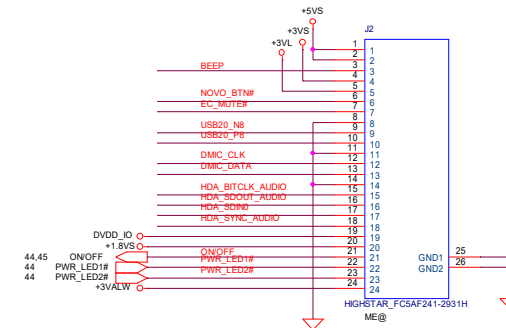
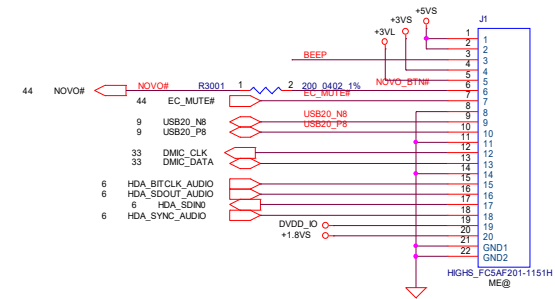
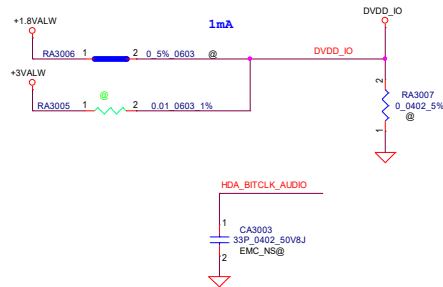
PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



CPU HDA BUS power 1.8VALW




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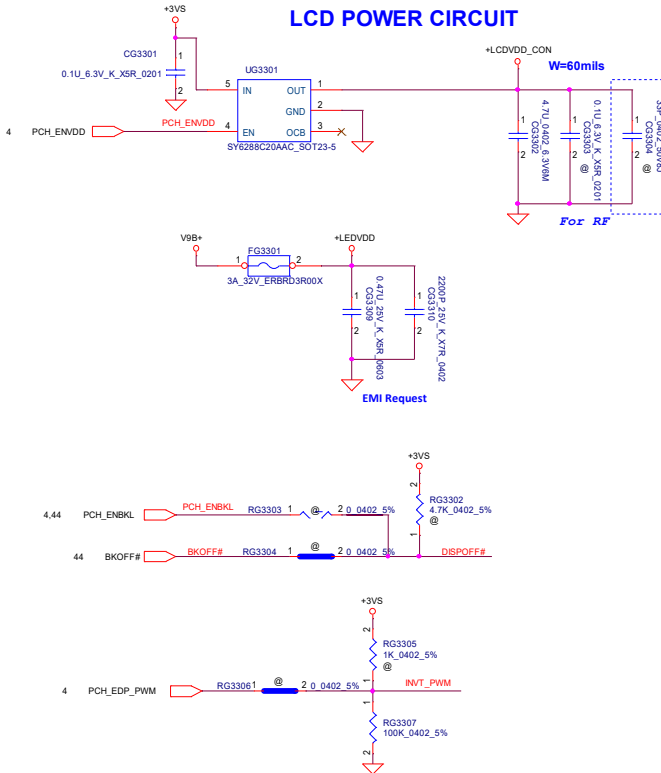
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Size	Document Number				Rev
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Date:		Friday, December 06, 2019	Sheet	31	of 60



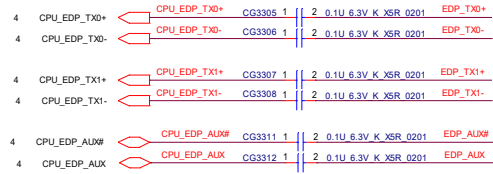
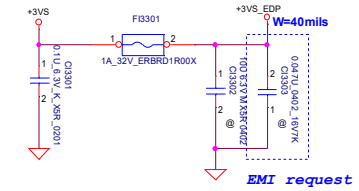
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C	GS44D/GS54D					0.1	
Date:		Friday, December 06, 2018		Sheet	32	of	60

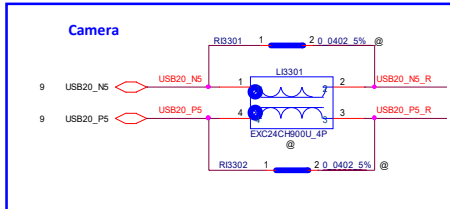
LCD POWER CIRCUIT



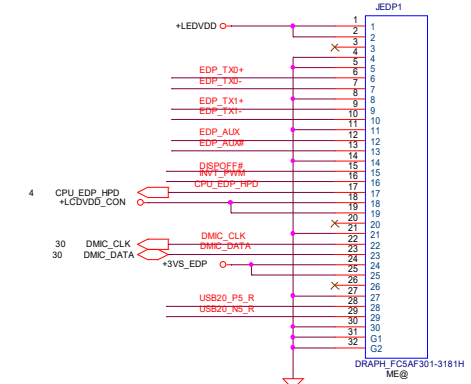
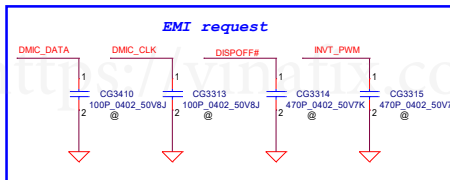
CMOS Camera



Camera

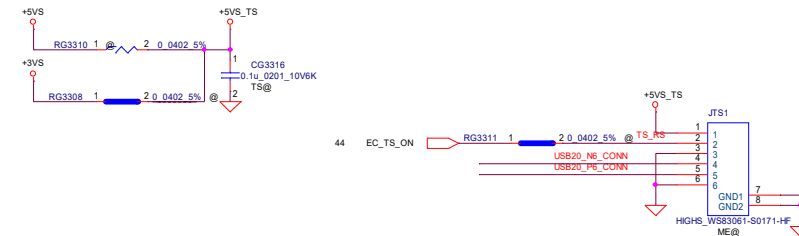
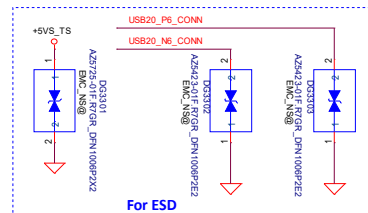
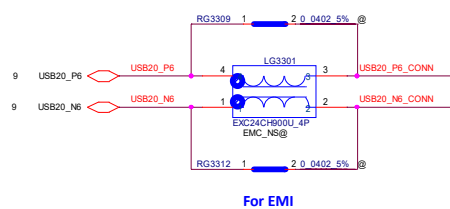


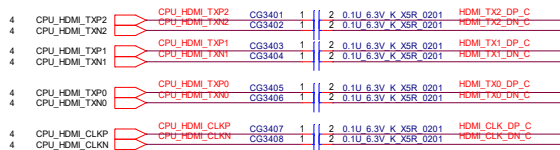
EMI request



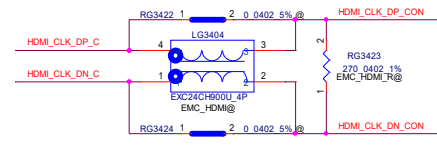
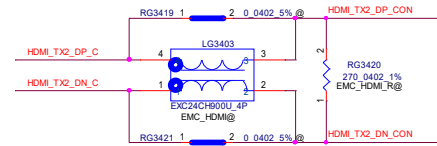
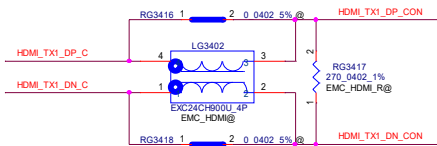
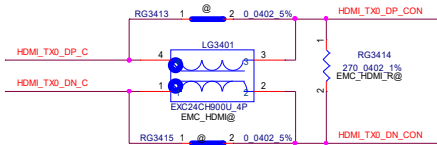
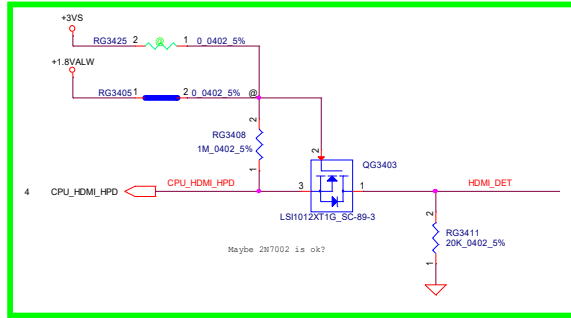
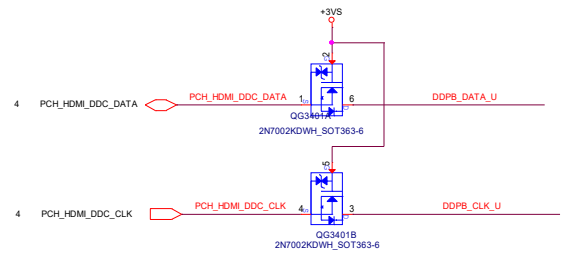
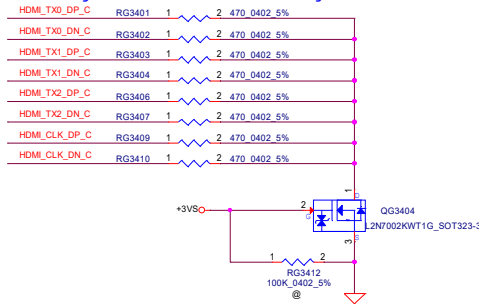
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Touch Screen

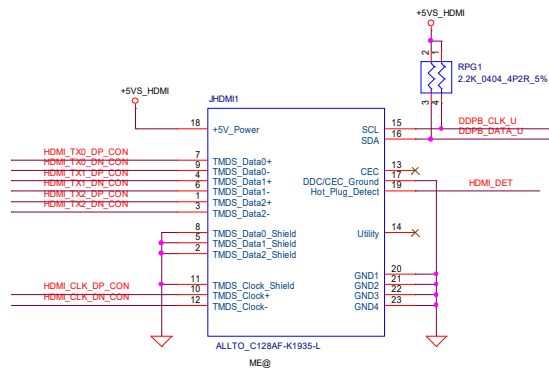
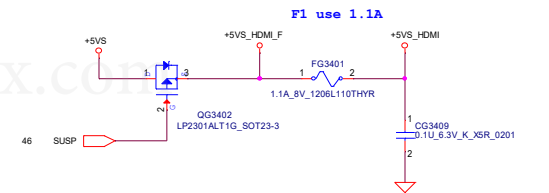
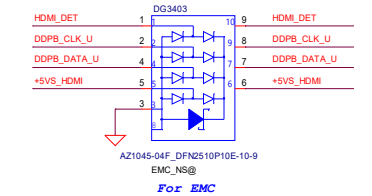
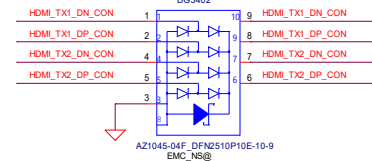
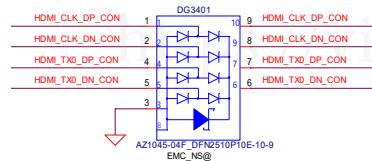




Need to change about 4700hm 5%-575412 Page115 Rev0.8



For EMC



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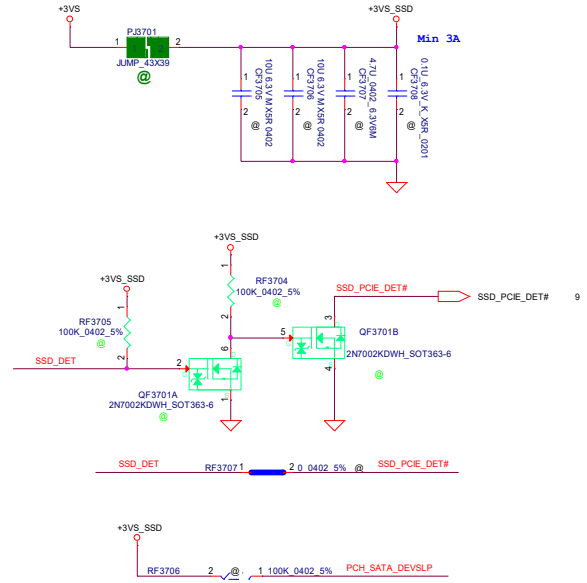
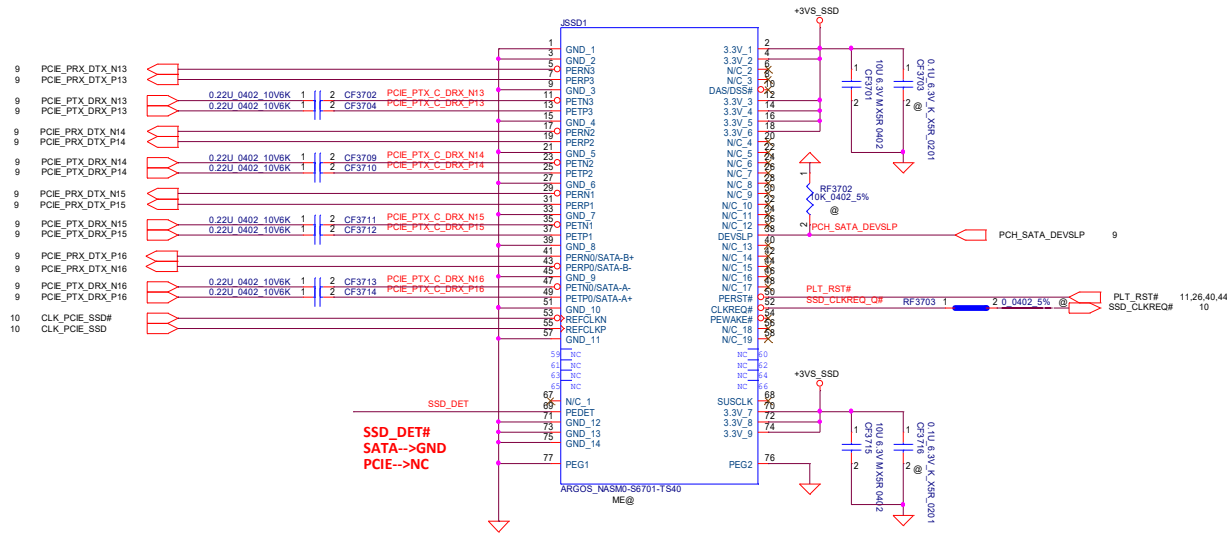
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				Date:	Friday, December 06, 2016
				Sheet	36 of 60
				Rev	0.1

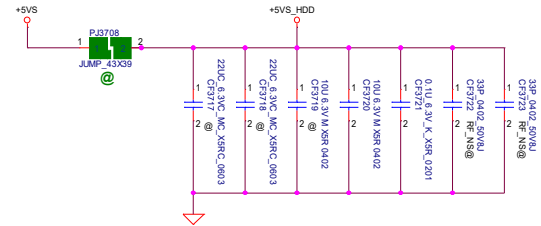
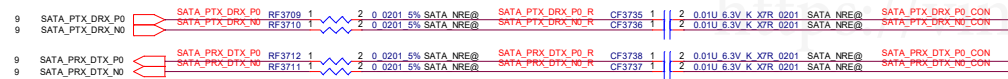


M.2 SSD

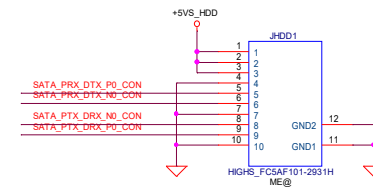
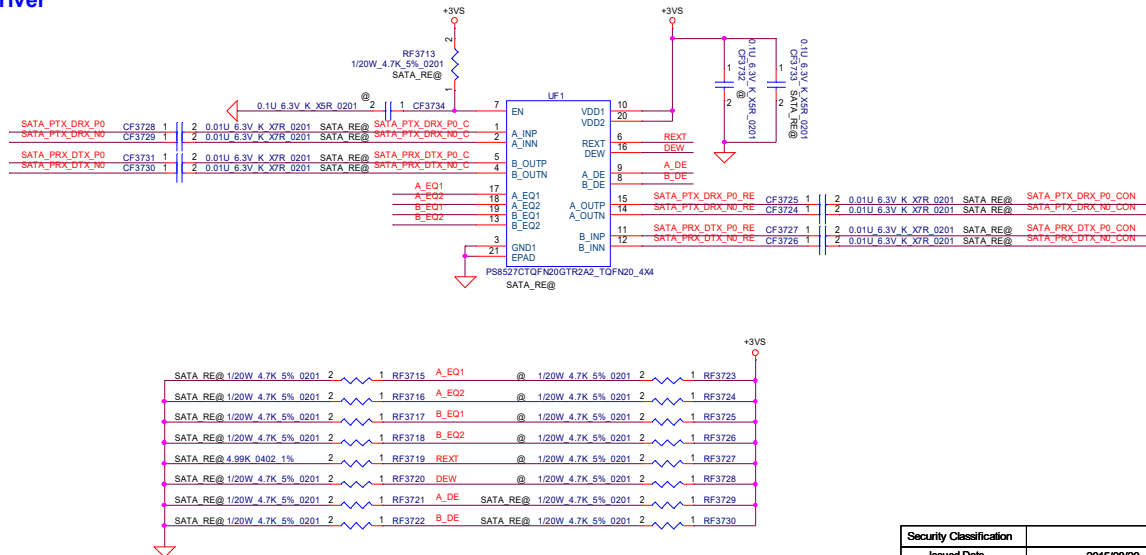
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SATA




SATA Redriver

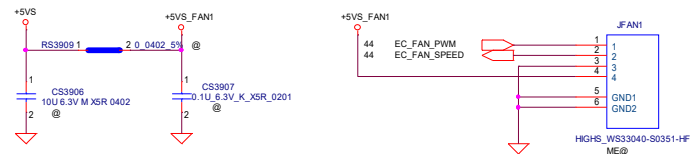
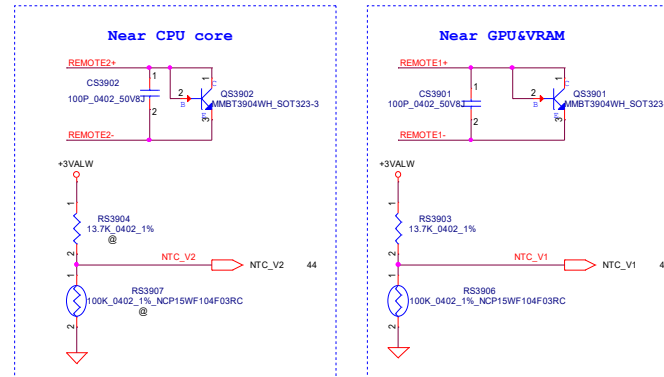
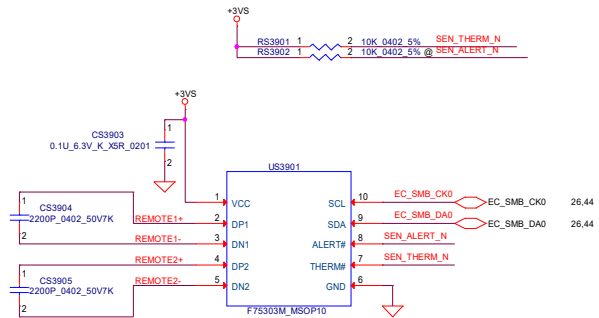



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2015/08/20		2016/08/20			
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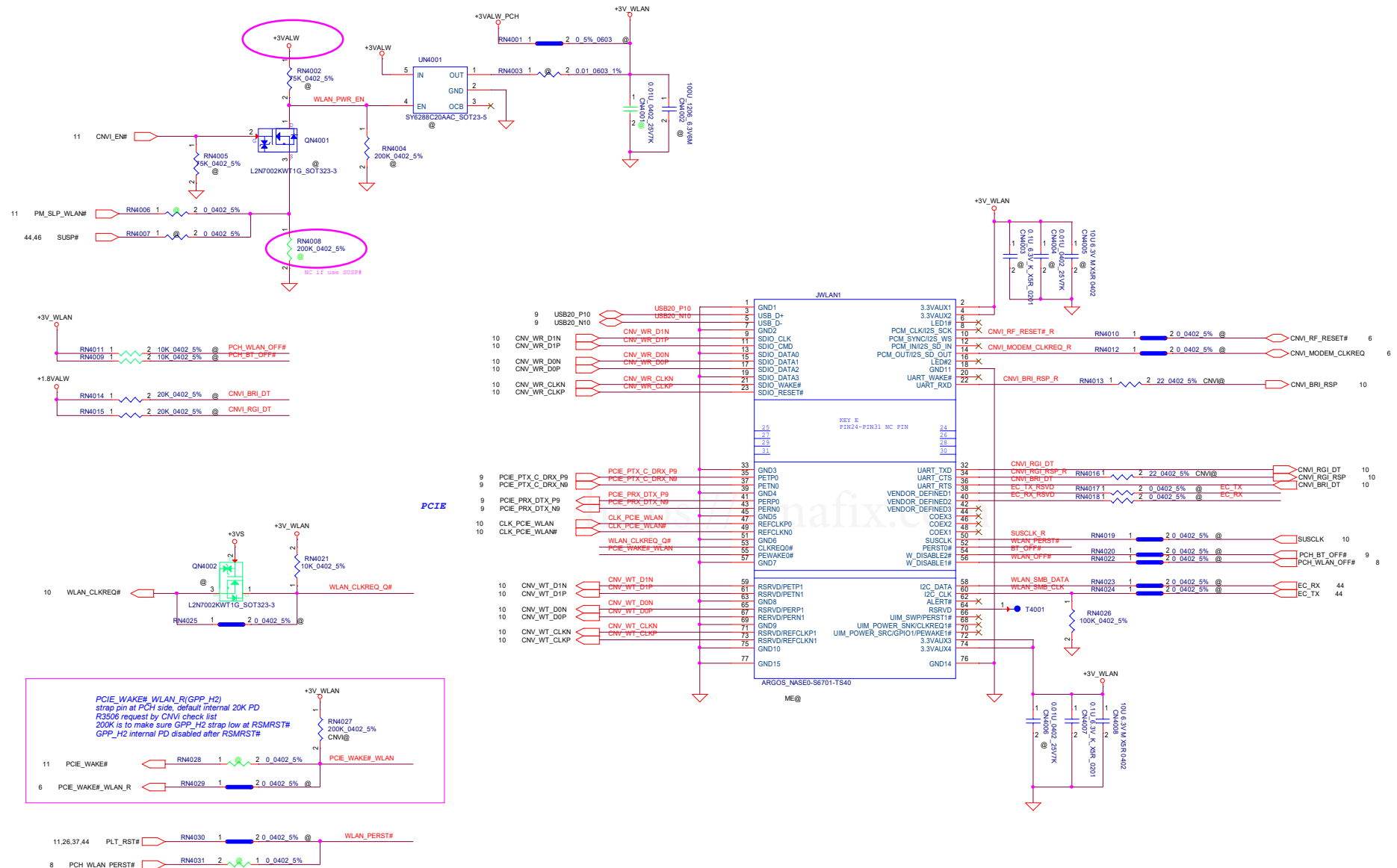
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Issued Date		2015/08/20	Deciphered Date	2016/08/20	SATA HDD CONN
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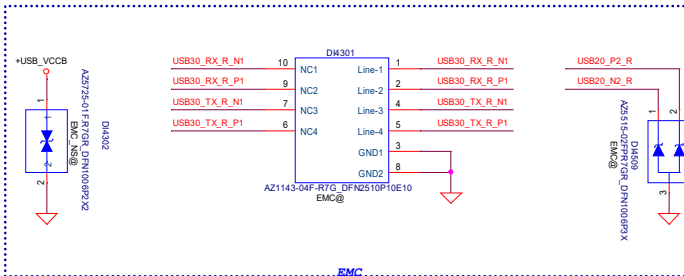
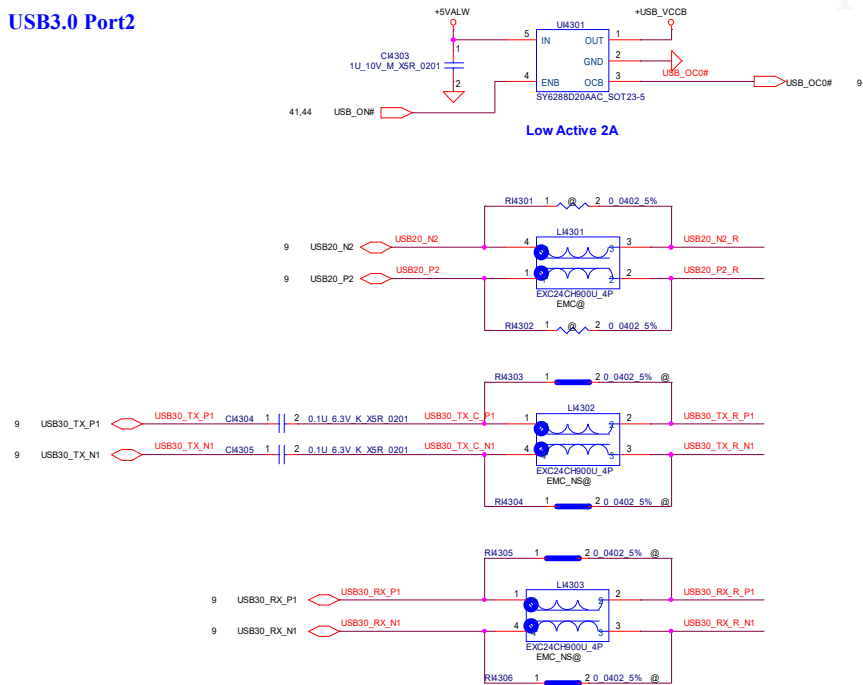
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Issued Date	2016/08/16	Deciphered Date	2017/08/15	Thermal sensor/FAN CONN.		
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Mini-Express Card(WLAN/WiMAX)



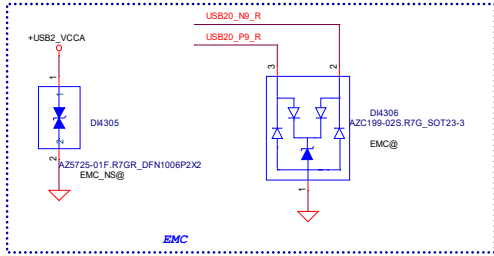
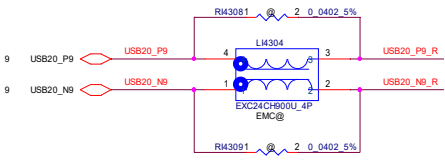
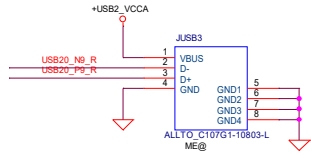
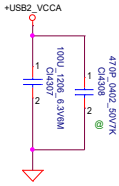
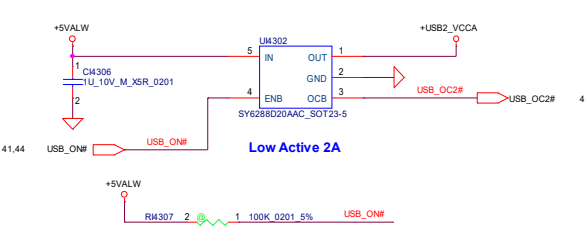
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USB3.0 Port2



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USB2.0 PORT x1



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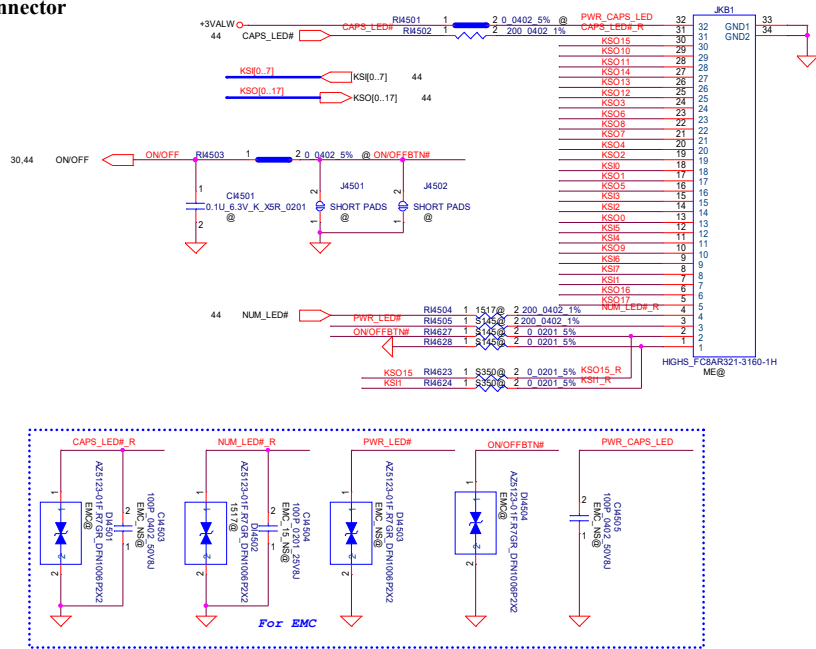
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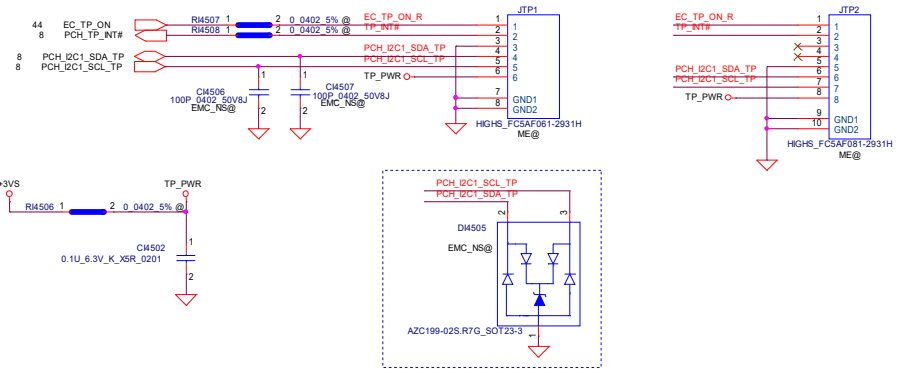
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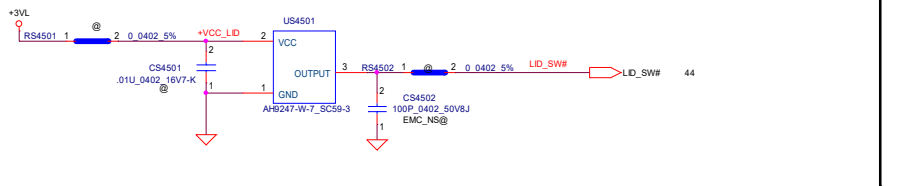
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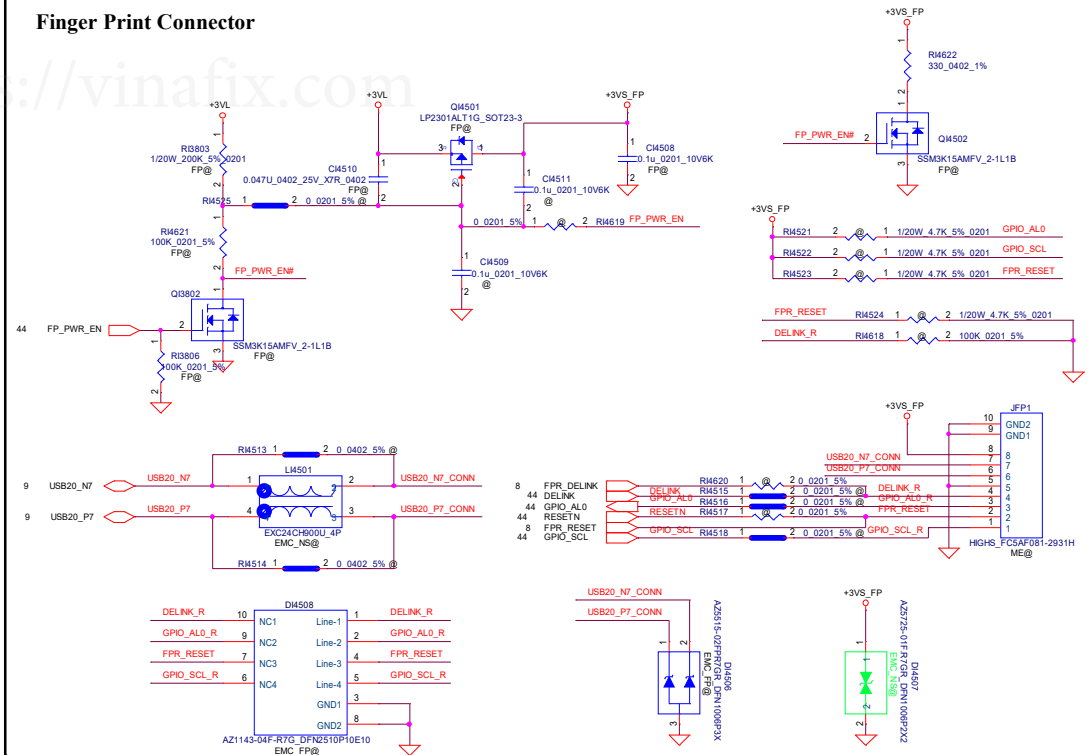
TP/B Connector



HALL Sensor




Finger Print Connector

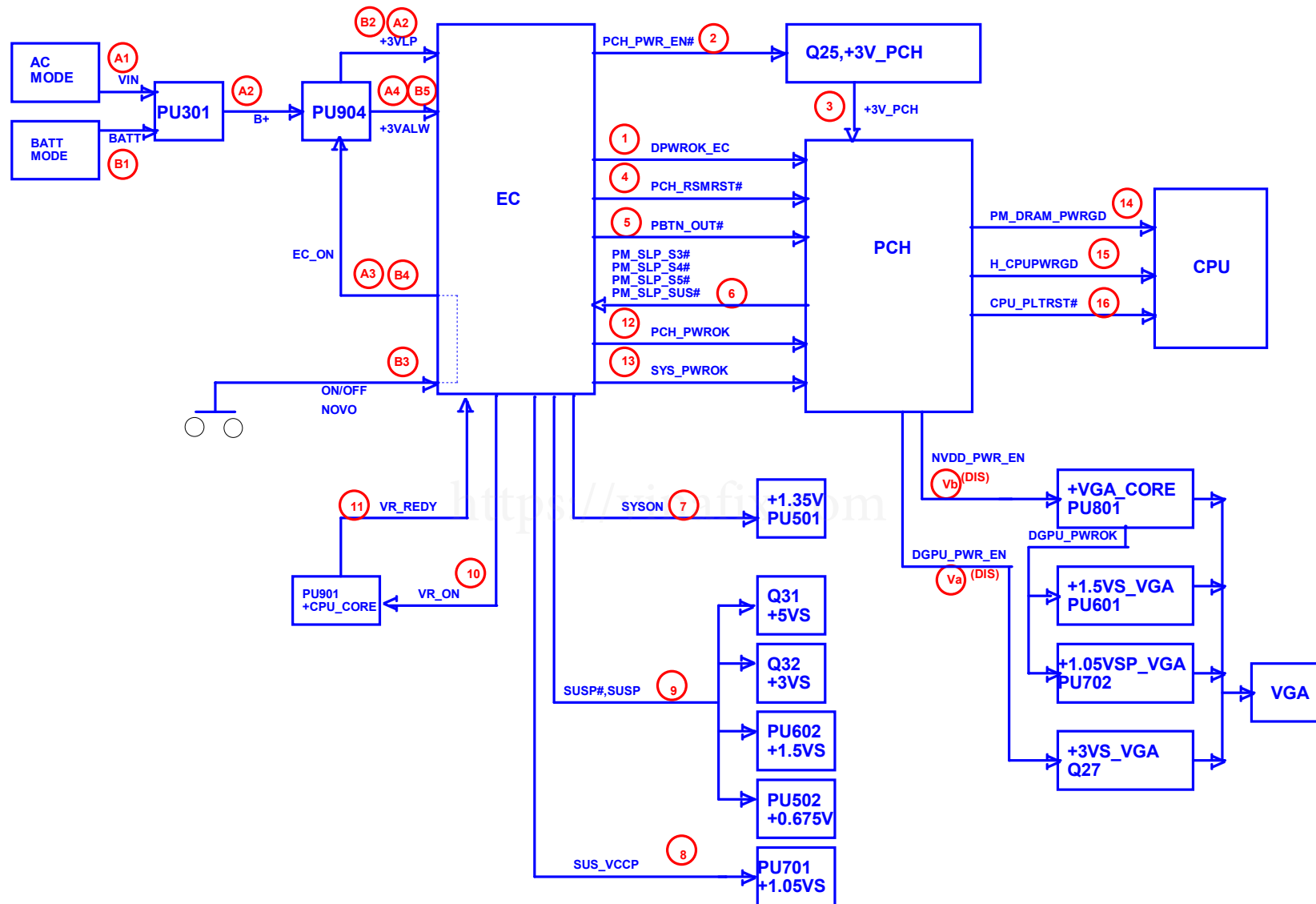


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The schematic illustrates the PMIC control logic for the MC74VHC1G32DFTT1G OR gate. It features two inverters, QX4602A and QX4602B, both PJT7838_SOT363-6. The input VCCST_OVERRIDE is connected to the inputs of both inverters. The output of QX4602A is connected to the input of QX4602B. The output of QX4602B is connected to the input of the OR gate (MC74VHC1G32DFTT1G). The output of the OR gate is connected to the input of the OR gate (MC74VHC1G32DFTT1G). The output of the OR gate is connected to the input of the OR gate (MC74VHC1G32DFTT1G).

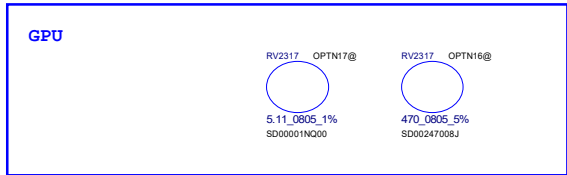
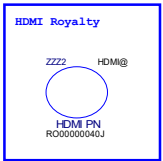
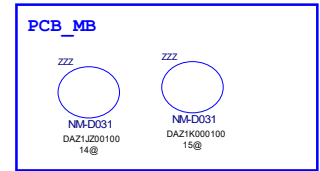
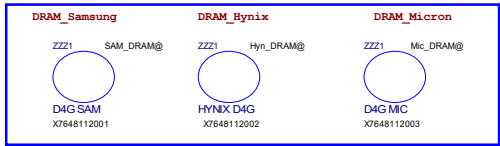
The image shows a PCB layout for a G2898KDIU_TDFN14P_2X03 component. The top section is a detailed view of the component footprint, showing pins 1 through 15. Pin 1 is connected to +5VALW, pin 2 to C177 (1u_0402_6.3V6K), pin 3 to C3916 (01U_0402_16V7-K EMC), pin 4 to +3VALW, pin 5 to +5VALW, pin 6 to C178 (1U_0402_6.3V6K), pin 7 to +3VALW, pin 8 to +3VLS, pin 9 to +3VLS, pin 10 to C173 (1 2200P_0402_25V7-K), pin 11 to C174 (0.1u_0201_10V6K), pin 12 to C176 (1 1000P_0201_50V7-K), pin 13 to +5VLS, pin 14 to J12 (JUMP_43X79), and pin 15 to Thermal Pad. The bottom section shows a 3V3V regulator circuit with R64, R27, C180, and C179.

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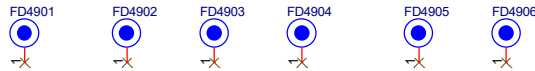
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Title		Power sequence block		
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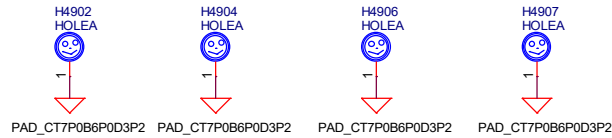


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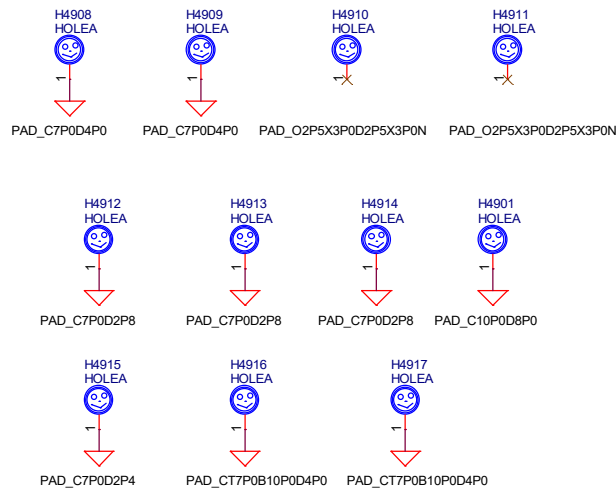
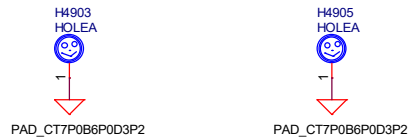
PCB Federal Mark PAD



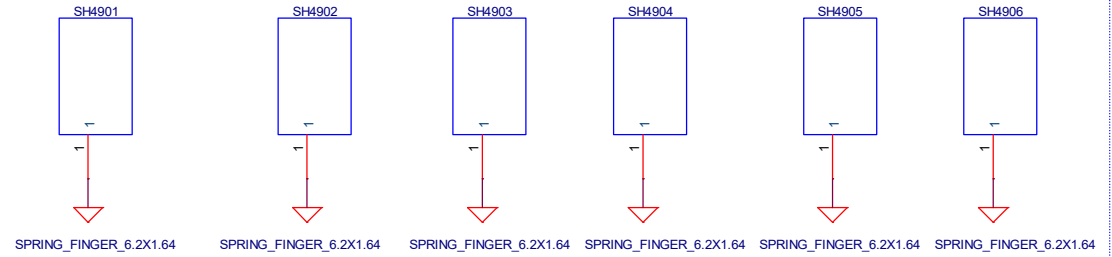
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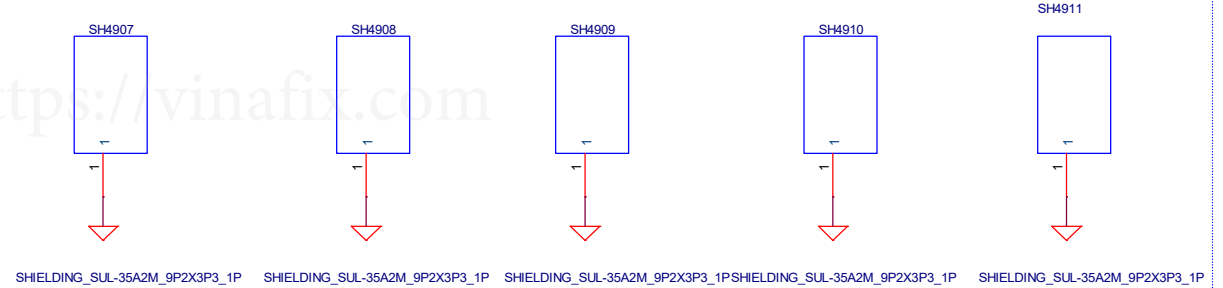
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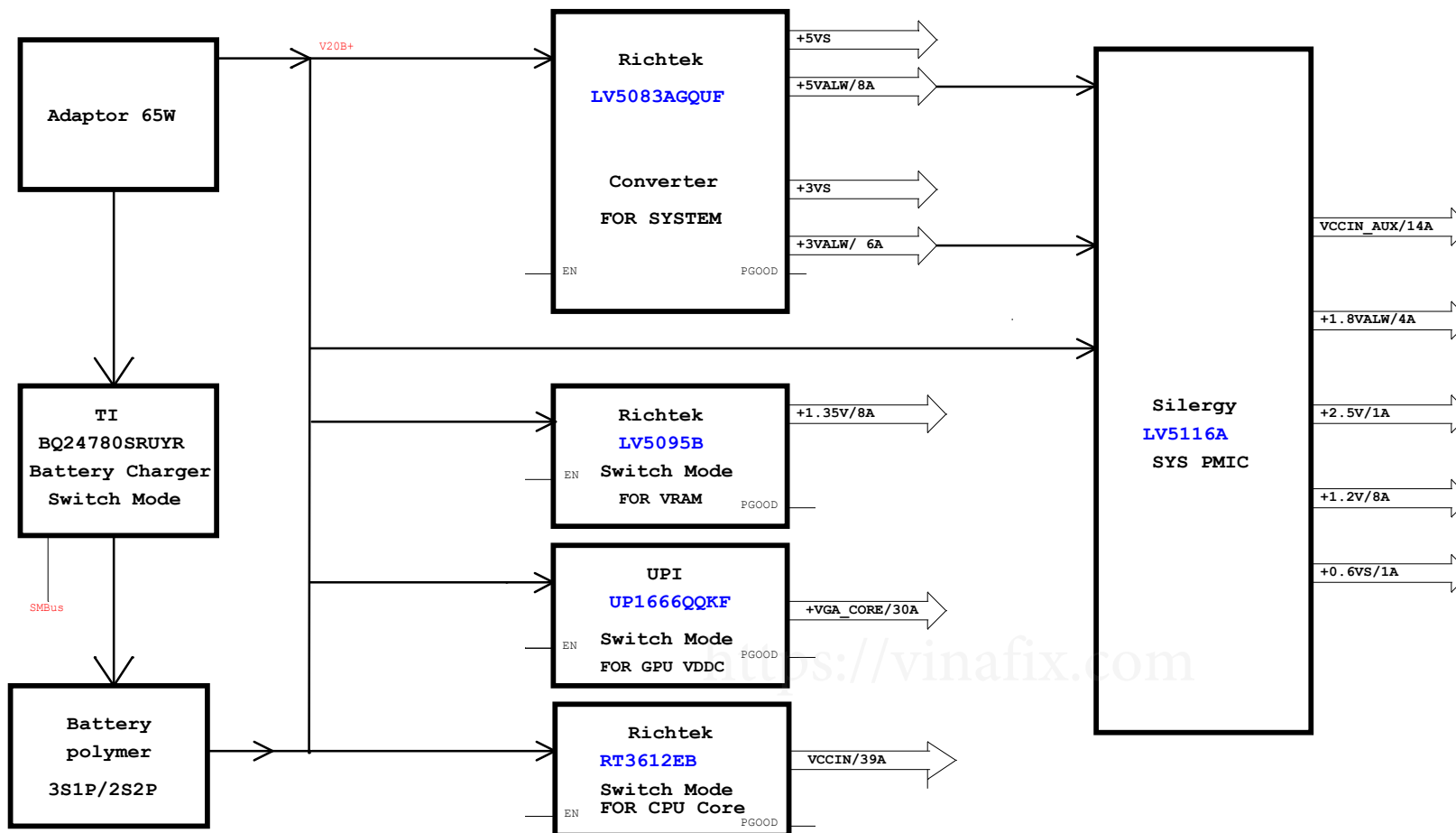
MD Shielding

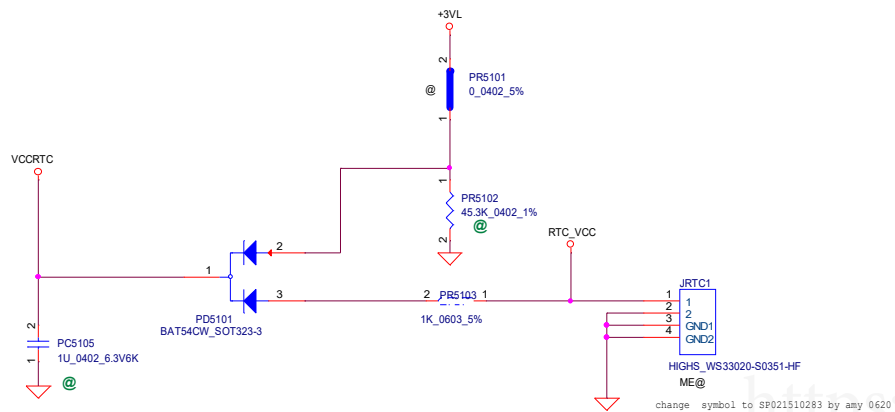
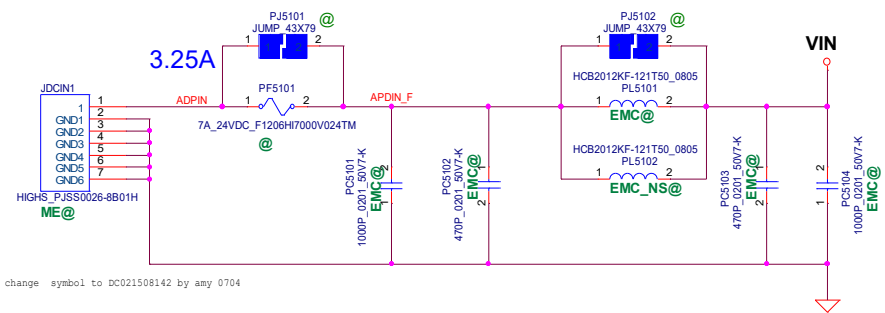


SODIMM Shielding



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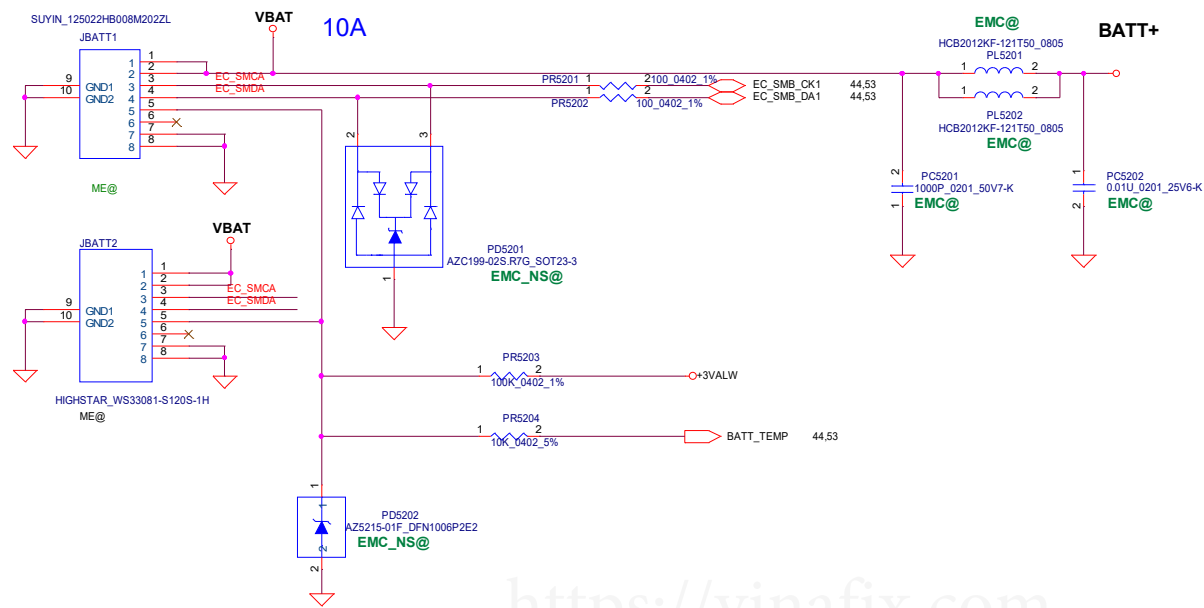




RTC_VCC 20MIL
+3V_L 20MIL
VCCRTC 20MIL

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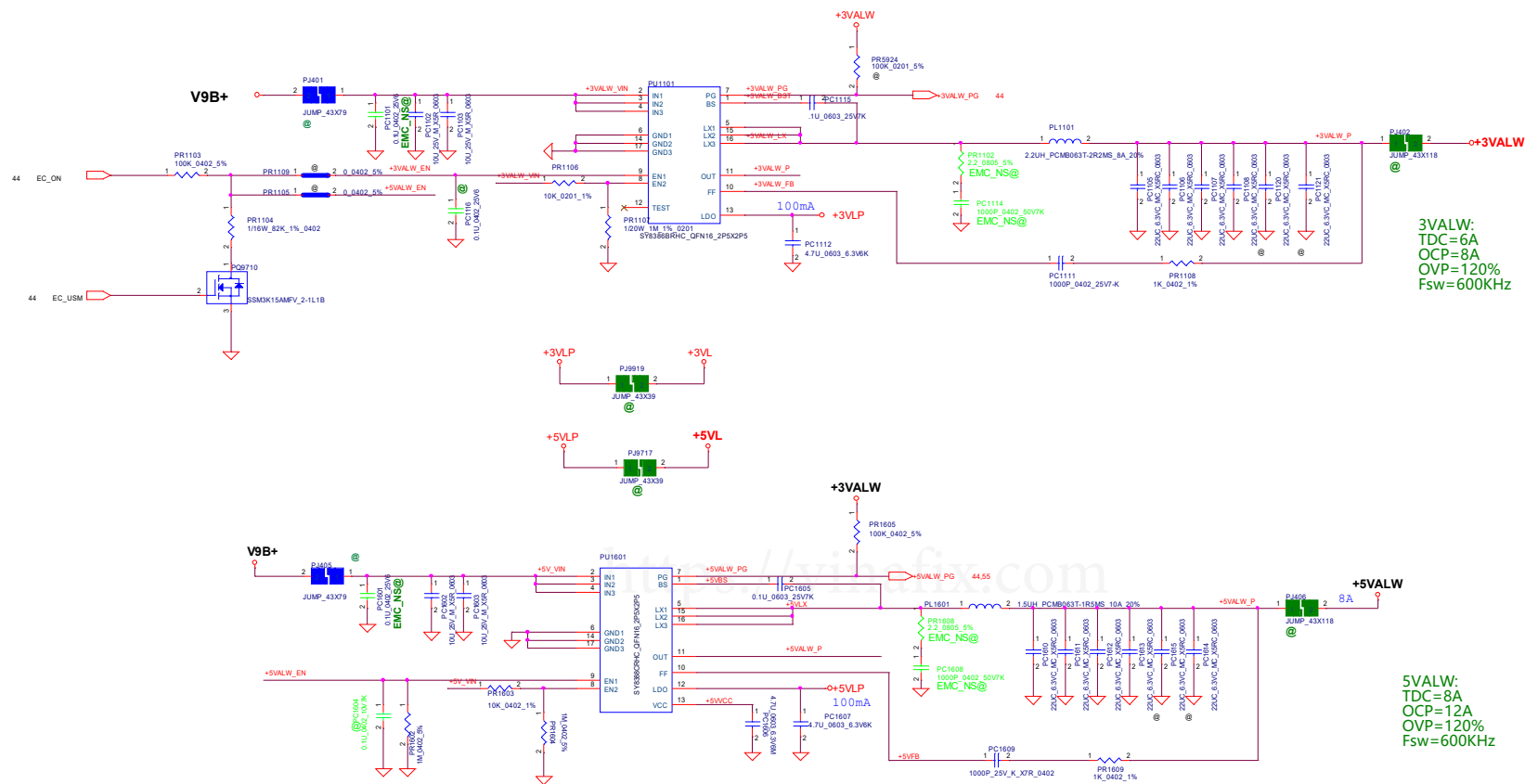
Security Classification	LC Future Center Secret Data			Title	PWR-DCIN / RTC charger	
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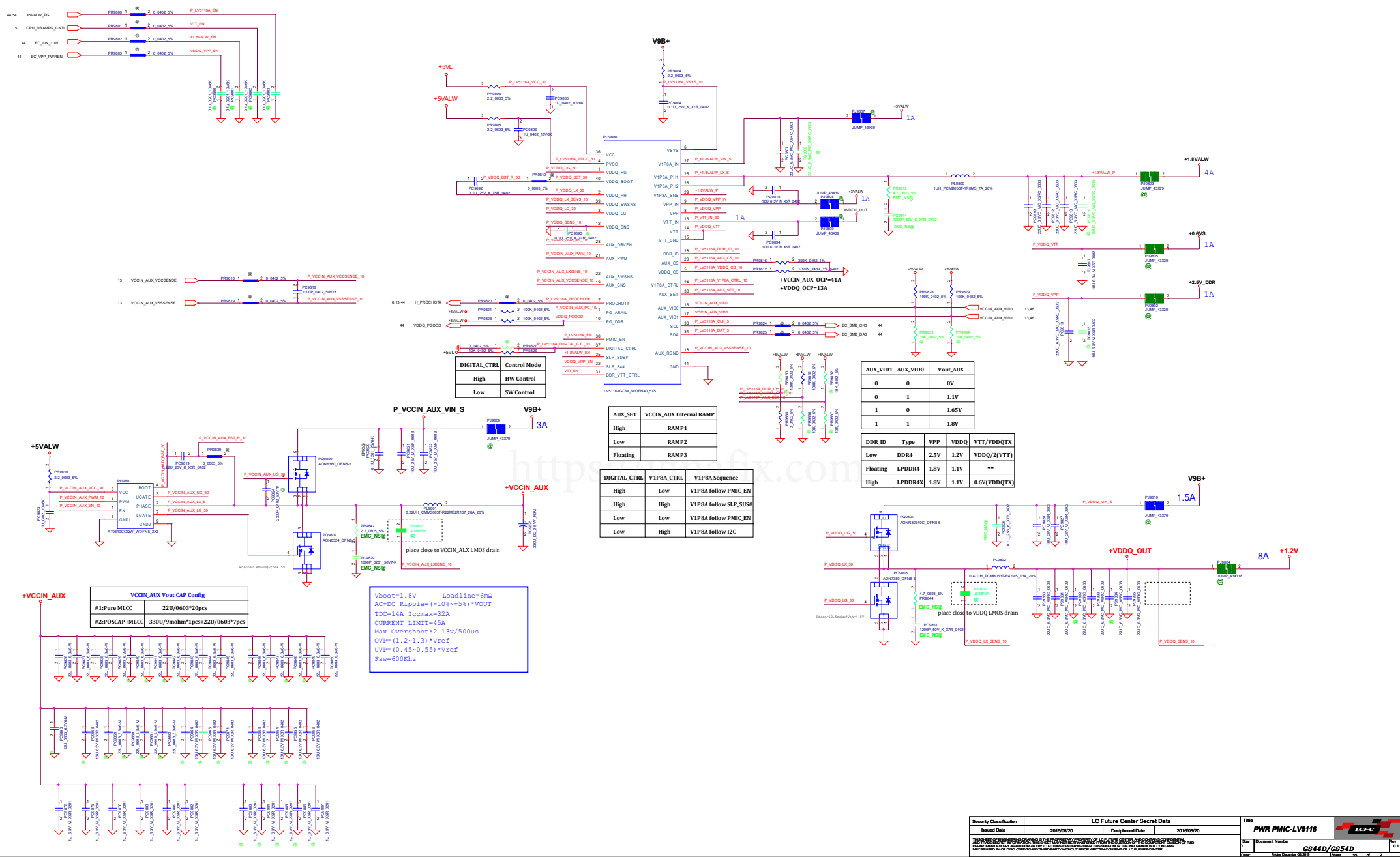


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POWER

U42@ PR3423 13.7K $\pm 1\%$ 0402 SD03413728J	U42@ PR3424 22.1K $\pm 1\%$ 0402 SD03422128J	U42@ PR3422 14K $\pm 1\%$ 0402 SD03414028J	U42@ PR3439 28K $\pm 1\%$ 0402 SD000015J00	U42@ PR3426 86.6K $\pm 1\%$ 0402 SD00001PM00	U42@ PR3432 24.9K $\pm 1\%$ 0402 SD03424928J	U42@ PR3434 1.18K $\pm 1\%$ 0402 SD00001D000	U42@ PR3438 29.4 $\pm 1\%$ 0402 SD00001BC00
U22@ PR3423 20.5K $\pm 1\%$ 0402 SD03420528J	U22@ PR3424 25.6K $\pm 1\%$ 0402 SD03425528J	U22@ PR3422 11.5K $\pm 1\%$ SD03411528J	U22@ PR3439 24.3K $\pm 1\%$ SD000011300	U22@ PR3426 130K $\pm 1\%$ 0402 SD03413038J	U22@ PR3432 22.6K $\pm 1\%$ 0402 SD000019W00	U22@ PR3434 1.1K $\pm 1\%$ 0402 SD03411018J	U22@ PR3438 40.2 $\pm 1\%$ 0402 SD034402A8J

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